AUTO-TUNING OF DIGITALLY CONTROLLED SINGLE-PHASE LOW HARMONIC RECTIFIERS AND INVERTERS

by

SUNG WOO MOON

B.S., Hongik University, Seoul, Korea, 2006

M.S., University of Colorado at Boulder, 2010

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has been approved for the
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_____
Prof. Dragan Maksimović

_____
Dr. Miguel Rodríguez González

Date_____

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Auto-tuning of Digitally Controlled Single-Phase Low Harmonic Rectifiers and Inverters

Thesis directed by Prof. Dragan Maksimović

Effective power transfer has been one of the main issues in power electronics. In particular, low-harmonic alternating current (AC) shaping is required by various regulations at the interface between AC power grid and direct current (DC) loads or sources,. In order to meet rapidly evolving efficiency standards and environmental concerns, intelligent AC current shaping strategies are required. In the power converter stage, however, inherent uncertainties caused by passive component tolerances and changes in operating conditions may impair the control loop stability, while mis-detection of operating modes over wide load range aggravates the situation further. This thesis introduces an auto-tuning technique in digitally controlled single-phase AC-DC rectifiers and DC-AC inverters. The approach is capable of precise on-line estimation of the power stage passive component values. The control loop compensator parameters are modified adaptively to maintain the nominal stability margins and control loop bandwidth based on the estimated component values. Furthermore, accurate continuous conduction mode (CCM) and discontinuous conduction mode (DCM) boundary detection is achieved as a result of the tuning process, without the need for additional circuitry. Implementation of the tuning approach is relatively simple. The proposed tuning approach is verified on experimental AC-DC and DC-AC prototypes.

Acknowledgement

My sincere gratitude to my Lord, my savior, Jesus Christ “Even though I walk through the valley of the shadow of death, I will fear no evil, for you are with me”

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Chapter 1

Introduction

Due to growing concerns related to energy savings and environmental issues, the standards for power electronics applications are becoming tighter both in efficiency and performance. The energy interface between a consumer and the utility is not one way anymore but rather interactive as distributed generation resources such as rooftop photovoltaic power systems become more common. Because of the different types of sources, effective power conversions from alternating (AC) power to direct current (DC) power and vice versa are essential in the power flow, as shown in Fig 1.1.

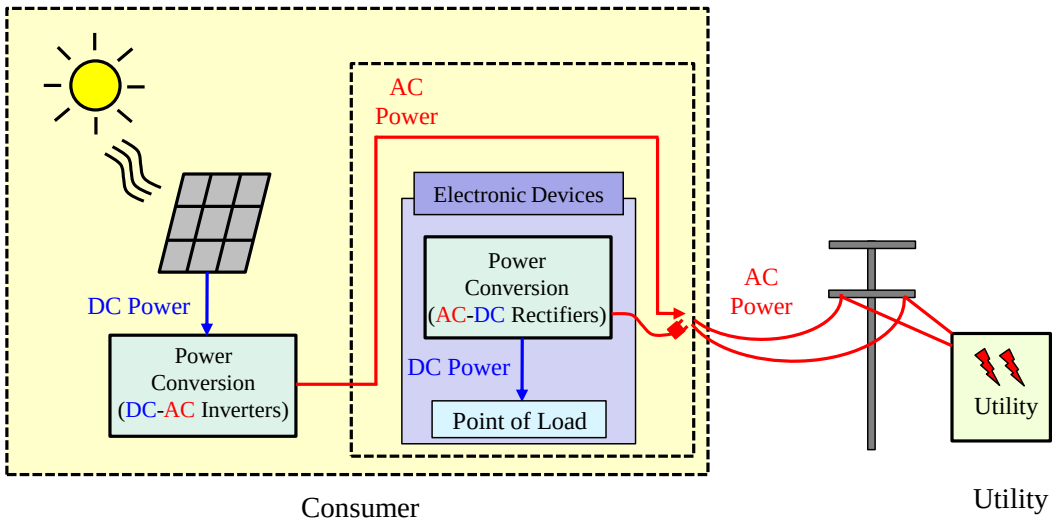


Fig 1.1. Power flow between consumer and utility

In electronic devices, AC-DC rectifiers are the first platform to receive AC power. The AC-DC rectifiers convert the input AC power into DC power, followed by DC-DC converters that perform voltage level shifting and point-of-load regulation as needed. The primary concern of converting the AC power into the DC power is not just to simply balance the power flow, but to perform the conversion efficiently and in a controlled manner. Specifically, AC current shaping is required to achieve low AC current harmonics and near unity power factor. Harmonics and phase shift of the AC input current with respect to the input voltage pollutes the AC distribution and reduces the power factor, thus degrading the power transfer performance. As a result, a rectifier capable of drawing sinusoidal input current in phase with sinusoidal AC voltage is one of the main specifications for an AC-DC rectifier.

In 2001, European Union (EU) put a standard EN-61000-3-2 in effect to limit the harmonic content of the rectifier input current, thereby finalizing the transition of AC-DC rectifier topology from conventional passive forms to more effective solutions [1]. Moreover, the increasing worldwide market volume accelerates the needs for more advanced rectifying topologies meeting the harmonic and power factor requirements.

Photovoltaic (PV) power systems are now becoming more popular due to decreasing costs and various incentives [2]. Price per watt for a PV module has now decreased to about 1.85~2.2 USD in 2009 from 4.4~7.9 USD in 1992. The total value of business in 2009 among the participant countries in the International Energy Agency Photovoltaic Power Systems Programme (IEA PVPS), which was founded in 1993 for the research and development of the photovoltaic solar energy, has reached

approximately 30 billion USD in 2009. Accordingly, there is increasing interest in grid-tied inverter systems interfacing PV modules and residential loads or the AC grid. In this respect it is worthwhile to develop robust, reliable inverter systems.

This thesis discusses and proposes an advanced power conversion module control technique with the specific focus on a digital auto-tuning technique for high power factor and low current harmonics in both single-phase AC-DC rectifier and DC-AC inverter systems, for effective power transfer between the grid and the consumer in the presence of power stage parameter tolerances and variations in operating conditions.

Chapter 2 presents a summary of single-phase AC-DC rectifiers, and introduces the general issues present in the system, which motivates the thesis research.

In Chapter 3, continuous-time domain power stage modeling for AC-DC rectifiers, and standard analog control techniques to regulate the input current and the output voltage are given.

Chapter 4 describes discrete-time modeling of the AC-DC power stage, details of digital controller implementation, as well as practical design examples. Nominal operation of the AC-DC rectifier system is verified on a 300 W prototype interfaced with the digital controller implemented on a Virtex-4 FPGA development board.

Chapter 5 introduces a novel auto-tuning technique for digitally controlled AC-DC rectifiers. The proposed control technique derives from unique characteristics of the power stage dynamics. Experimental results verify the proposed approach in a prototype operating over the universal input voltage range.

Chapter 6 further improves the system operation over the wide load range using power stage parameters attained from the auto-tuning technique. Accurate conduction mode detection of continuous conduction mode (CCM) and discontinuous conduction mode (DCM) enables a two-mode compensator where the parameters are switched adaptively according to the detected mode. Consequently, the high power factor and low current harmonics are achieved over a wide range of loads.

Chapter 7 extends the auto-tuning technique to single-phase grid-tied DC-AC inverter systems, taking advantage of the similarities between grid-tied DC-AC inverter and AC-DC rectifier power stage dynamics.

Chapter 8 concludes the thesis and summarizes the contributions.

Chapter 2

AC-DC Boost Power Factor Correction (PFC) Rectifiers

This chapter introduces fundamentals of single-phase AC-DC rectifiers. In the AC-DC power conversion system, one of the most important objectives is to achieve high power factor and low current harmonics. As power factor decreases, the power distribution cost increases, and the energy loss during the power transmission will increase. Therefore, for the energy supplier point of view, it is highly beneficial if the consumer end maintains the high power factor and low current harmonics. Thus, the appropriate standards or guidelines for AC-DC rectifier performance are required.

European standard EN-61000-3-2 specifies the limit of the individual current harmonic contained in the AC input current [1]. Table 1.1 shows specific harmonic

Table 2.1: EN61000-3-2 harmonic current limits for Class D equipment

Harmonic Order n	Maximum Permissible Harmonic Current per watt mA/W	Maximum permissible harmonic current A
3	3.4	2.30
5	1.9	1.14
7	1.0	0.77
9	0.5	0.40
11	0.35	0.33
13≤n≤39 Odd harmonics only	3.85/n	0.15 15/n

Table 2.2: Power factor guidelines for Energy Star and 80 Plus Program

Load %	**Energy Star**			**80 Plus Program**			
	Silver	Gold	Platinum	Bronze	Silver	Gold	Platinum
10%	0.65	0.65	0.65	-	-	-	-
20%	0.80	0.80	0.80	-	-	-	-
50%	0.90	0.90	0.90	0.90	0.90	0.90	0.95
100%	0.95	0.95	0.95	-	-	-	-

current limits for personal computers, computer monitors, and television receivers.

Recently, more enhanced energy saving programs are emerging, and pushing the AC-DC power supply manufacturers to acquire higher qualifications [3]-[5]. US government-backed Energy Star program claims the different minimum power factors over a wide range of loads as specified in Table 2.2 [3].

A utility organization Northwest Energy Efficiency Alliances (NEEA) also funded 80 Plus program to encourage power supply companies to improve the efficiency and power factors of AC-DC power supplies for computers. In order to qualify the Platinum in 80 Plus program, at least 0.95 power factor is required [4]. Apparently, it is becoming more desirable to qualify higher labels to be competitive in the industry.

In this chapter, the power factor is defined in Section 2.1. The typical rectifier topologies are addressed and compared in Section 2.2, while Section 2.3 explains the basic operation of boost DC-DC converter employed in the AC-DC power factor correction rectifiers. The motivation of the research will be presented in the last section.

2.1 Power Factor

Regardless of efficiency, the energy produced by a source is not completely transferred and consumed by the load in the power form conversion systems such as AC-DC rectifiers or DC-AC inverters. Depending on the AC current shape and phase shift respect to the AC voltage, some degree of energy circulation between the source and the load occurs and therefore degrades the energy transfer performance of the system. The circulating energy is not physically lost through power processing, though it does not do any real work. In this sense, power factor (PF) measures how effectively the energy, which does the real work, is transferred from the source to the load in the system. Simply, the power factor is,

$$Power\ Factor\,(PF) = \frac{Average\ Power}{(rms\ voltage)\times(rms\ current)} \tag{2.1}$$

The power factor varies from 0 to 1. Assuming that the source voltage is purely sinuosoidal, as harmonics included in the AC current increase, the denominator in (2.1) increases, and the phase shift between the AC voltage and the AC current increases, the nominator in (2.1) decreases.

Intuitively, it is required to remove the harmonics in the AC current, and the AC current should be in phase with the AC voltage to maximize the power factor. In the AC-DC rectifiers, for example, the energy transfer effectiveness depends completely on the composition of the load. When the source voltage is purely sinusoidal and the load is purely resistive, then the power factor is unity value. If the load consists of energy storage components, such as inductors and capacitors, the transferred energy from the source is stored in the form of electric or magnetic fields

in the load and returns back to the source. Thus, this returned energy does not contribute to the net energy flow from the source to the load. This term is called displacement factor. The displacement factor can be represented as

$$Displacement\ Factor = \cos\theta_{iv} \tag{2.2}$$

θ_{iv} represents the phase difference between the AC voltage and AC current. Non-linear loads, such as rectifiers, distort the shape of input current, resulting in undesired input current harmonics. These harmonics also do not increase the net energy transfer from the source to the load. This term is called distortion factor, which is the ratio of the RMS current of fundamental component to the total RMS current.

$$Distortion\ Factor = \frac{\frac{I_1}{\sqrt{2}}}{\sqrt{I_o{}^2 + \sum_{n=1}^{\infty} \frac{I_n{}^2}{2}}} \tag{2.3}$$

Therefore, another way to define the power factor is

$$Power\ Factor = (Distortion\ Factor) \times (Displacement\ Factor)$$

$$= \frac{\frac{I_1}{\sqrt{2}}}{\sqrt{I_o{}^2 + \sum_{n=1}^{\infty} \frac{I_n{}^2}{2}}} \cdot \cos\theta_{iv} \tag{2.4}$$

It is equivalent expression to (2.1). Equation (2.4) clearly shows how the current harmonics and phase shift penalize the power factor. For unity power factor, it is required to make the AC current in phase with AC voltage, and remove the undesired harmonics included in the AC current.

2.2 AC-DC Power Factor Correction (PFC) Rectifiers

The majority of electronic devices require DC power from an AC supply. Universal input voltage ranging from 85 to 265V_{rms}, with a line frequency of 47Hz~63Hz should be rectified and re-scaled adaptively according to the specific applications requirements. For example, computer microprocessors require a supply

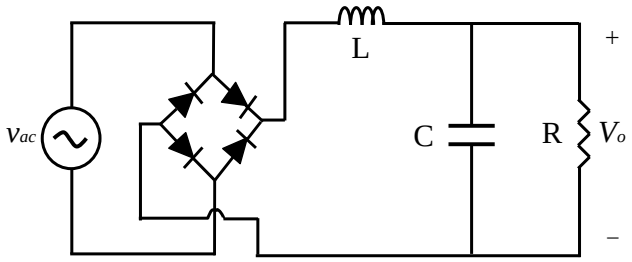


Fig 2.1. Passive AC-DC rectifier

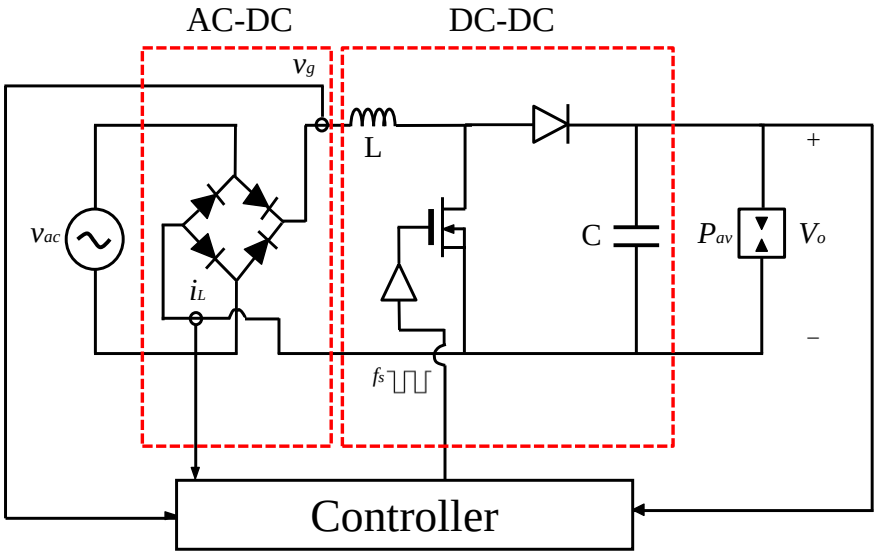


Fig 2.2. Active power factor correction (PFC) rectifier

voltage equal to or less than 1 DC voltage from the universal AC input power. The first task of power processing modules from front to end is the rectification of AC power into DC power. AC-DC rectifiers determine how effectively this task is fulfilled.

AC-DC rectification circuits are classified into two groups, passive AC-DC rectifiers and active AC-DC power factor correction (PFC) rectifiers. Even though the passive rectifiers are simple, inexpensive and exhibit reliable performance, it is not an adequate solution for current application standards due to relatively high line current harmonics, low power factors. Even if the filter component values are adjusted as required to achieve high power factor and low current harmonics, it is not the best solution due to large sizes of the passive elements.

The active AC-DC rectifiers, whereas, show extremely low current harmonics and almost perfect power factors as well as small passive element sizes. In the DC stage, feedback controlled dc-dc converters are employed for the purpose of regulating tight output voltage, power balance, and current shaping.

Fig 2.3 illustrates the ideal behavior of active AC-DC rectifiers. Since one of main objectives of the active AC-DC power factor correction rectifiers is maintaining the power factor as unity value, it is required that the circuit model seen from the AC input side should be modeled as a purely resistive load. Then, the AC input voltage is always in phase with the input current and proportional in amplitude. This resistive load, so called emulated resistance (R_e), is not an actual resistance but behaves like a resistor. It makes the input AC current shape emulates the input AC voltage shape by following Ohm's law. At the same time, this emulated resistance R_e transfers the AC

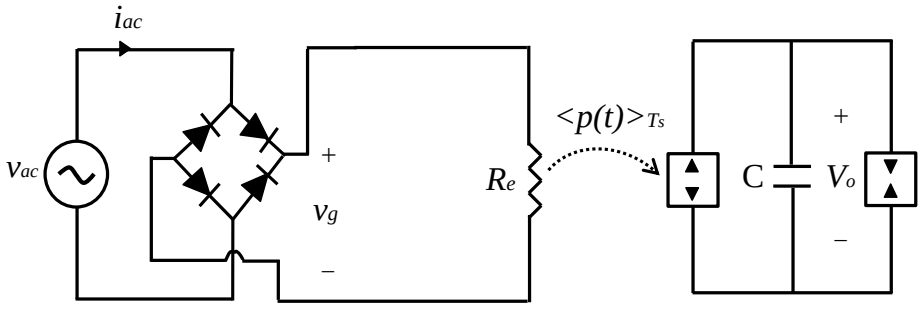


Fig 2.3. Ideal behavior of active PFC rectifier

input power to the DC output port. Virtually consumed power by this emulated resistance will be completely transferred to the output port, balancing the input and output power. In consequence, for optimized performance of the active AC-DC rectifiers, the control technique of the DC-DC converter inserted in the active AC-DC rectifiers plays the most important role.

2.3 DC-DC Boost Converter

DC-DC boost converter is the most widely used topology for active power factor correction rectifiers. Basically, any converter topologies such as the buck-boost, SEPIC, and Cúk converters, which are capable of producing input-to-output conversion ratios varying from 1 to infinity can be employed in the PFC applications. Among them, the boost converter exhibits the least switch device stress and highest efficiency. The typical output voltage regulated through the boost converter is around

400 DCV. Thus, it is necessary to grasp the large signal characteristics of the DC-DC boost converter for intuitive understanding of active PFC rectifiers.

2.3.1. Continuous Conduction Mode (CCM)

The DC-DC boost converter circuit is shown in Fig 2.4. The pulse signal applied to the transistor Q is called the switch driving signal. During one switching period T_s, Q is on when pulse is high (dT_s), and the diode D is on for the rest of switching period $(1\text{-}d)T_s$. Then, the given inductor voltage and capacitor current for the time interval dT_s, when Q is on, are

$$v_L = V_g \tag{2.5}$$

$$i_c = \frac{-v_o}{R} \tag{2.6}$$

During time interval $(1\text{-}d)T_s$, when the diode D is on,

$$v_L = V_g - v_o \tag{2.7}$$

$$i_c = i_L - \frac{v_o}{R} \tag{2.8}$$

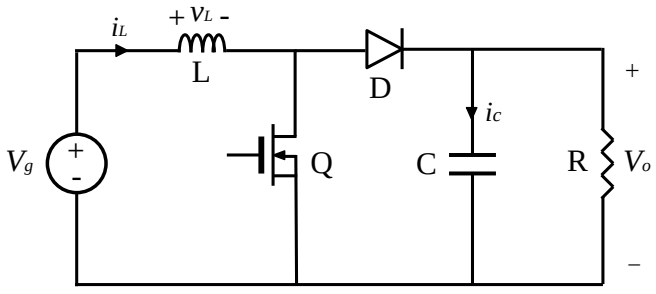
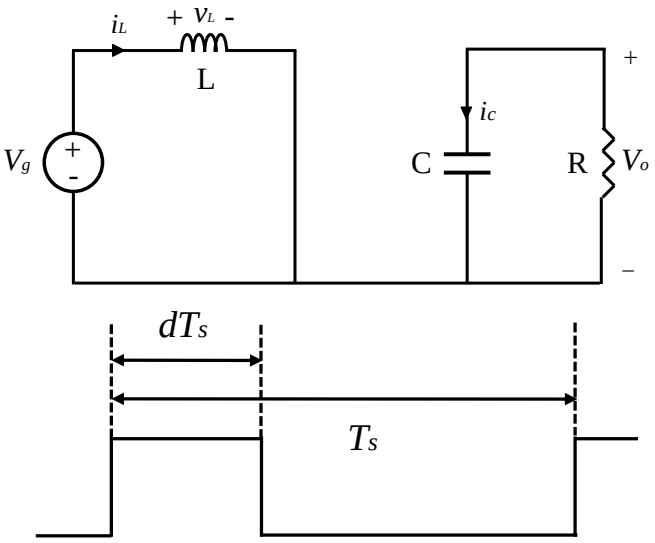
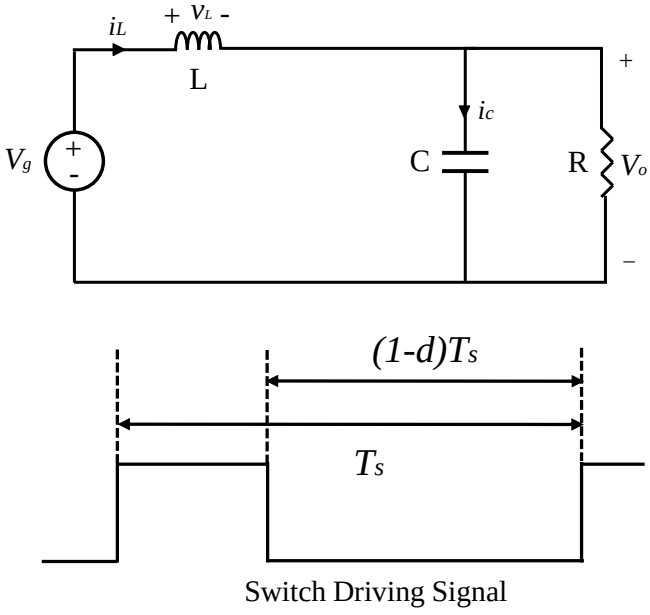


Fig 2.4. DC-DC boost converter



Switch Driving Signal

(a) Subinterval 1: when MOSFET conducts



Switch Driving Signal

(b) Subinterval 2: when diode conducts

Fig 2.5. Boost converter switching

If it is assumed that the ripple on the inductor current and output capacitor voltage is negligible, it is possible to approximate $v \approx V, i_L \approx I$. Then, total volt-seconds balance applied to the inductor, and net change of the capacitor charge for a single switching period are respectively ,

$$\int_0^{Ts} v_L(t)dt = V_g(dT_s) + (V_g - V_o)(1-d)T_s \tag{2.9}$$

$$\int_0^{Ts} i_c(t)dt = (\frac{-V_o}{R})(dT_s) + (I - \frac{V_o}{R})(1-d)T_s \tag{2.10}$$

In steady state, the total volt-seconds balance applied and the net change in capacitor charge over one switching period are both zero. Finally, it becomes

$$V_g = (1-d)V_o \tag{2.11}$$

$$I = \frac{V_g}{(1-d)^2 \cdot R} \tag{2.12}$$

Since the duty cycle *d* varies from 0 to 1, the ability to regulate the output voltage to be greater than the input voltage is verified in the equation (2.11).

2.3.2. Discontinuous Conduction Mode (DCM)

In this operating mode, during time interval 2, the inductor current comes down to zero before the next switching cycle starts. In this case, since the current cannot conduct backward through the diode, both switches, the MOSFET and diode, are turned off for some fraction of the time period. This situation happens when the inductor current ripple is larger than the average inductor current. This mode is called discontinuous conduction mode (DCM). An Extra converter operation state, the 3rd state, is added to CCM case as illustrated in Fig. 2.6.

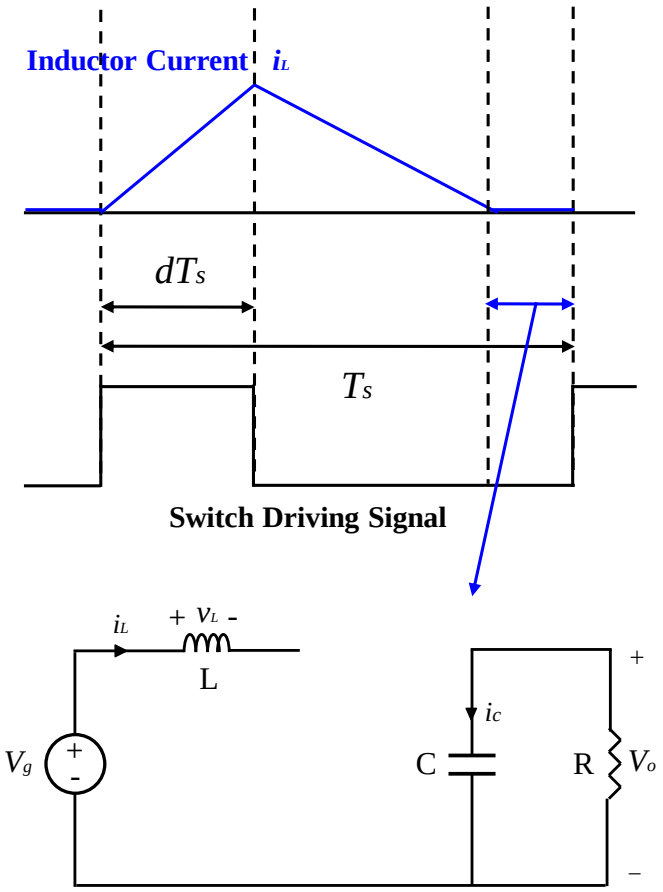


Fig. 2.6. 3rd subinterval for discontinuous conduction mode (DCM)

$$v_L = 0 \tag{2.13}$$

$$i_c = \frac{-v_o}{R} \tag{2.14}$$

In DCM, deriving the input-to-output voltage conversion ratio is not as simple as in CCM, because the diode conduction time is not simply (1-*d*). It is needed to compute the charge under the diode current precisely and equate it to the output current, then solve it for diode conduction time. Finally it bocomes a quadratic equation, and ends up with the solution of,

$$\frac{V_o}{V_g} = \frac{1+\sqrt{1+\frac{4d^2 R \cdot T_s}{2L}}}{2} \tag{2.15}$$

Though this dc-dc boost converter DCM large signal characteristic (2.15) does not tell much about boost based PFC rectifiers operating in DCM. Nevertheless, it is worth understanding how the converter operates in DCM and shows different characteristics compared to the CCM operation.

2.4 Research Motivations

As shown in the previous sections, the boost converter based active power factor correction rectifier is currently the dominant topology for the AC-DC rectifier. As this active power stage topology becomes popular, control method applied to drive the switch in the DC-DC converter plays more important role correspondingly. Under any circumstances, the feedback controller should be implemented in such a way that the ideal rectifier behavior is achieved as in Fig 2.3.

Undesired controller operation, however, can occur due to unintended passive component parameter variations in the power stage or the controller. Especially, tolerances of power stage passive components tend to exert negative influences on the control loop characteristics by deviating from nominal operating conditions of the intended controller design. This will impair the loop stability margins, accordingly AC current shaping capability will be degraded. This could be the serious problem hard to deal with especially considering the rigorous standards, which currently requires at least 0.95 power factor for the highest label, and expected to be more tighter in the

future. In order to go along with the current ‘go green’ trend, even trivial defects present in the system will not be allowed.

In conclusion, it is required to develop a more advanced control scheme that maintains the desired operation as the system designer intended at the design stage despite the power stage uncertainties. Technically, on-line estimation of power stage passive component values should be the vital function, and the corresponding automatic control loop parameter adjustment is going to be core objective of the proposed approach in the thesis. The small add-on to the conventional controller with less effort will be the secondary consideration to enhance the value of the approach.

CHAPTER 3

Average Current Mode Controlled Power Factor Correction (PFC) Rectifiers

A number of control techniques have been developed for boost PFC rectifiers [6]-[8]. Among them, average current mode control method is one of the popular control methods for its reliability and operations over wide input voltage and power ranges [6]-[7]. Detailed average current mode control technique analysis and modeling are addressed in this chapter. In Section 3.1, analog average current mode control technique is addressed. Continuous time power stage modeling is presented in Section 3.2. The entire current and voltage control loop modeling is in Section 3.3, and the input voltage feedforward technique is introduced in Section 3.4.

3.1 Average Current Mode Control

Two feedback loops (current and voltage loops) are implemented for their own purposes. The current loop makes the input current track the shape of the input voltage, while the voltage loop controls the magnitude of emulated resistance, which directly controls the magnitude of input current. As shown in Fig 3.1, the averaged inductor current passed through the low pass filter should track the current reference

which changes with twice the line frequency. Since the current loop reference is a rectified and scaled version of the input voltage, the current loop reference contains a much higher frequency factor at the zero crossings of the ac input voltage as illustrated in Fig 3.2. Therefore, the current loop should have relatively high bandwidth (2~10kHz).

In the voltage loop case, it is required to maintain extremely low bandwidth (less than 10Hz). It only modifies the magnitude of emulated resistance in such a way that it balances the power of input and output side. This loop should work very slowly,

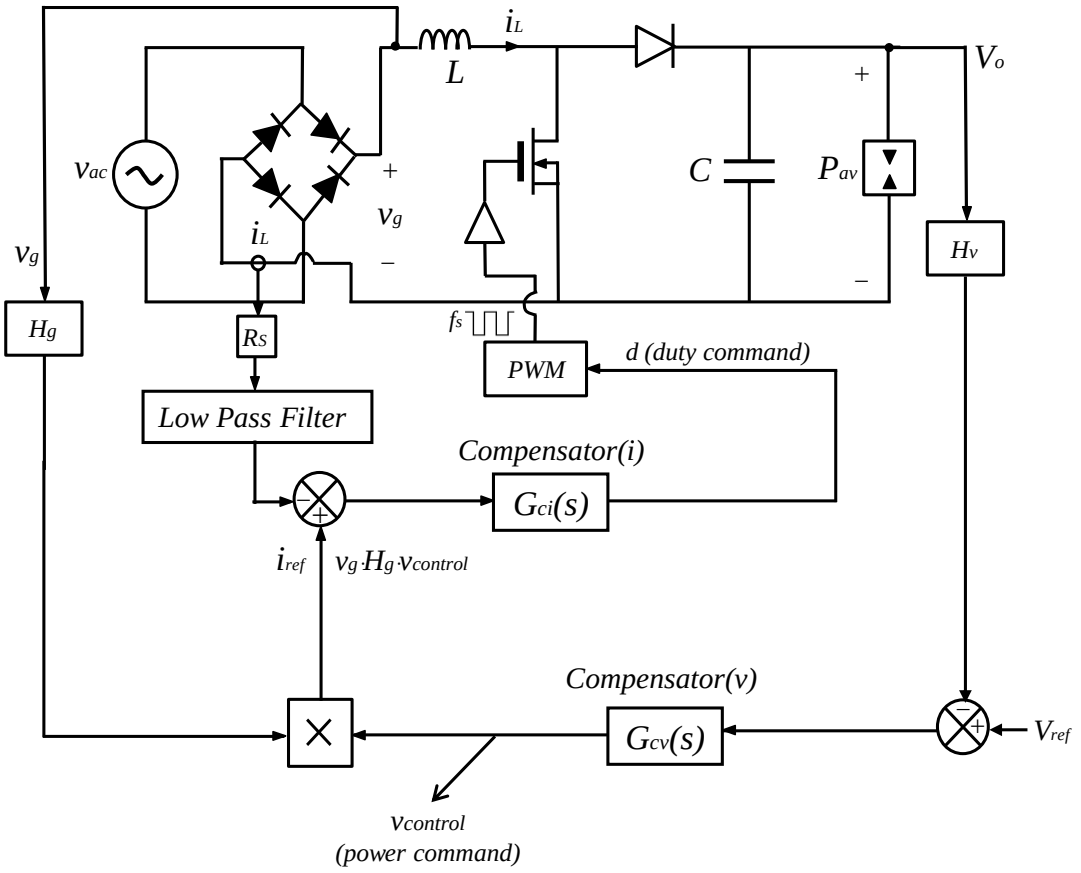


Fig 3.1. Average current mode controlled PFC rectifier

or it will inject the harmonics into the input current as shown in Fig 3.3 because it is one of the current loop reference components.

In summary, the current loop mainly shapes the input current, while the output voltage loop balances the power and regulates the output voltage as required.

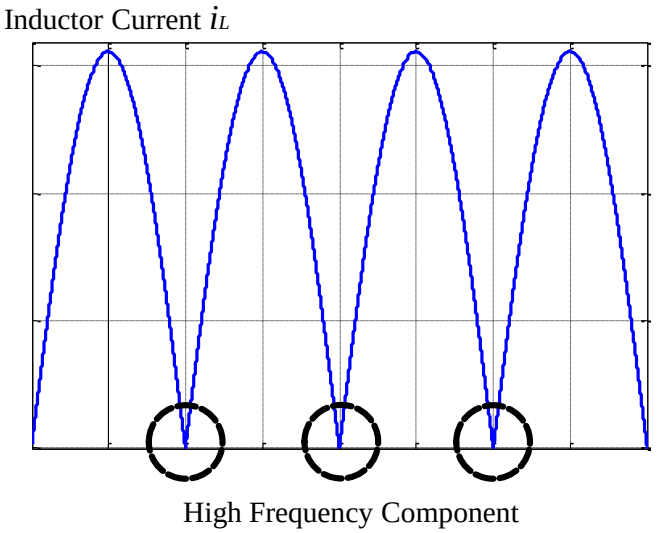


Fig 3.2. High frequency behavior of the current loop

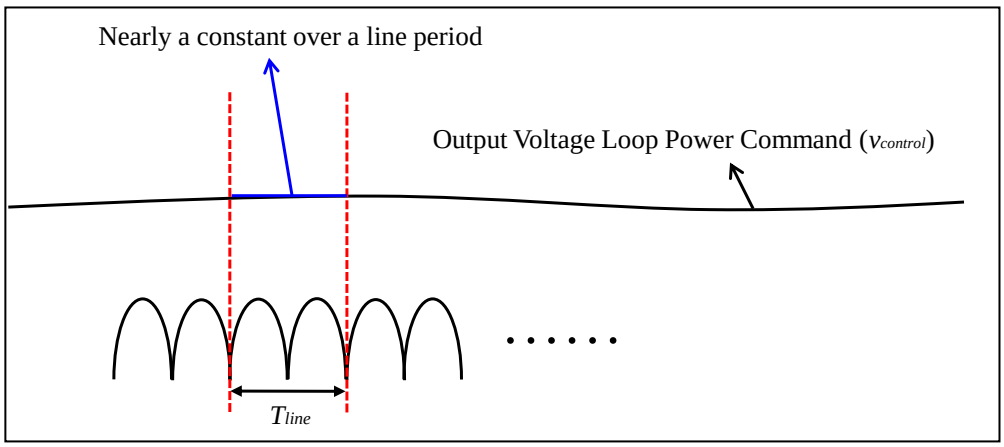


Fig 3.3. Low frequency behavior of the voltage loop

3.2 Modeling of Boost Power Factor Correction (PFC) Rectifiers

The power stage modeling is addressed in this section [9]-[11]. For average current mode control, it is desirable to model the small signal response of duty cycle(d) to inductor current(i_L), and power command ($v_{control}$) to output voltage(v_o) to accommodate the current and voltage loop design respectively. In the duty-to-inductor current response case, it is very important to note that some assumptions are need to be applied since the AC-DC boost converter itself is highly nonlinear due to varying input voltage and duty command. From the switching-period-averaged model in Fig 3.4, the inductor current equation can be constructed,

$$L\frac{d < i_L >_{T_s}}{dt} = < v_g(t) >_{T_s} - d'(t) < v_o(t) >_{T_s} \tag{3.1}$$

Where d' is 1-d. If the switching frequency(~100kHz) is much higher than line frequency(50~60Hz), every signal can be assumed to be constant over one switching period. The equation (3.1) is nonlinear and can be linearized only when there is an assumption that the small variations on the output voltage is way smaller than the large signal output voltage, i.e,

$$< v_o(t) >_{T_S} = V_o + \hat{v}_o(t) \tag{3.2}$$

$$\left|\hat{v}_o(t)\right| << \left|V_o\right| \tag{3.3}$$

Then, the small-signal nonlinear equation can be written as

$$L\frac{d\left\langle \hat{i}_L(t)\right\rangle_{T_s}}{dt} = \left\langle v_g(t)\right\rangle_{T_s} + d'(t)V_o + d'(t)\hat{v}_o(t) \tag{3.4}$$

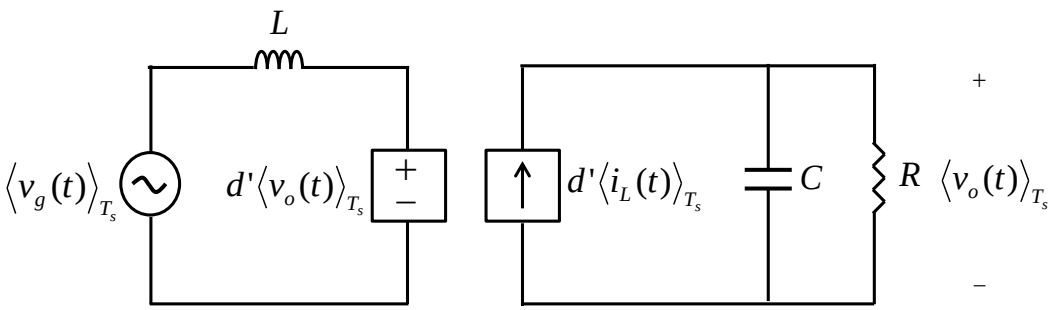


Fig 3.4. Large signal model averaged over switching period T_s

If the assumption (3.3) and linearization are applied to the above equation, the last term in the equation is much smaller than the other terms, and it is reduced to

$$L\frac{d\langle \hat{i}_L(t)\rangle_{T_s}}{dt} = \langle v_g(t)\rangle_{T_s} - d'(t)V_o \tag{3.5}$$

Finally the averaged duty-to-inductor current transfer function can be obtained by sending the line voltage signal to zero.

$$G_{id}(s) = \frac{i_L(s)}{d(s)} = \frac{V_o}{sL} \tag{3.6}$$

where $i_L(s)$ is the Laplace transform of $<i_L(T)>_{Ts}$.

The power command-to-output voltage transfer function start out from the ideal large-signal model in Fig 3.5. As it is addressed in the previous subsection, the output voltage loop bandwidth is extremely low (~1/10 of line frequency), the signals containing frequency components larger than the line frequency can be averaged and simplified, and finally the linearization results in the small signal model in Fig 3.6 with the coefficients of

$$j_2 = \frac{P_{av}}{V_o \cdot V_{control}} \tag{3.7}$$

$$r_2 = \frac{V_o^{\,2}}{P_{av}} \tag{3.8}$$

If it is assumed that the output load is pure resistor *R*, the control-to-output transfer function becomes,

$$G_{vc}(s) = \frac{\hat{v}_o}{\hat{v}_{control}} = j_2 \cdot R \| r_2 \frac{1}{1 + sCR} \tag{3.9}$$

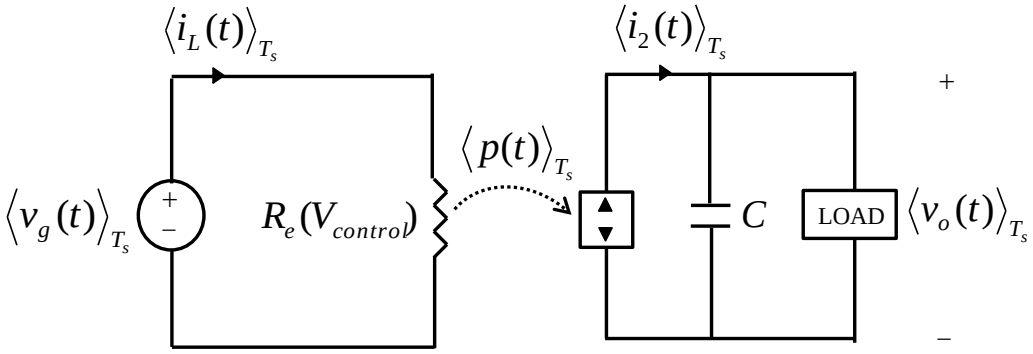


Fig 3.5. Large signal ideal rectifier model averaged over switching period T_s

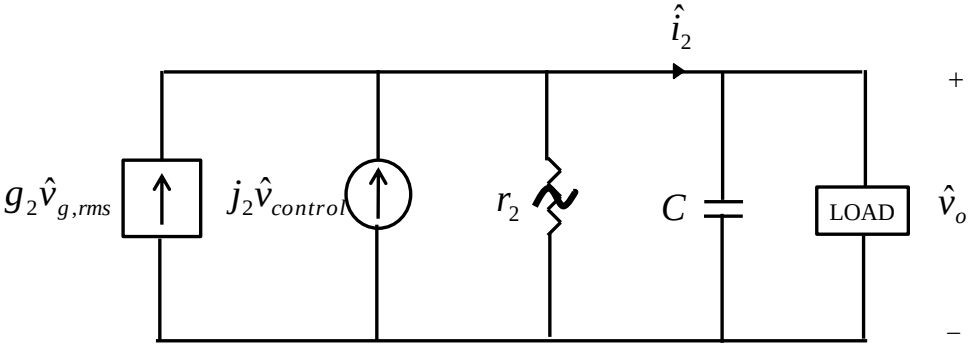


Fig 3.6. Small signal model

Since the transfer function (3.9) represents the case for the resistive load, it is required to obtain the expression when the output is loaded with a 2nd stage high bandwidth dc-dc converter, which is more likely the case. In this case, the second stage continuously draws the constant power, which can be modeled as a power sink, and this power sink, in turn, can be represented as negative resistance, which has the same magnitude with γ_2, but opposite polarity. It is quite reasonable because the increasing output voltage causes decreasing output current and vice versa to maintain the constant output power. This behavior is modeled as a negative resistor in incremental point of view. The control-to-output transfer function, therefore, becomes

$$G_{vc}(s) = \frac{\hat{v}_o}{\hat{v}_{control}} = \frac{j_2}{sC} = \frac{P_{av}}{V_o V_{control}} \cdot \frac{1}{sC} \tag{3.10}$$

3.3 Modeling of Average Current Mode Controlled PFC Rectifiers

For the compensator design and stable operations of PFC rectifiers, appropriate dynamic modeling of averaged current mode controlled PFC rectifiers is essential [6]. From the transfer functions diagram shown in Fig 3.7, two unique feedback loop gain expressions can be constructed.

$$\text{Current Loop Gain : } T_i(s) = G_{id}(s) \cdot R_s \cdot LPF(s) \cdot G_{ci}(s) \tag{3.11}$$

$$\text{Voltage Loop Gain : } T_v(s) = G_{vc}(s) \cdot H_v \cdot G_{cv}(s) \tag{3.12}$$

In the current loop gain, $G_{id}(s)$ represents the power stage control-to-inductor current transfer function, R_s is the inductor current sensing gain, $LPF(s)$ is the transfer function of low pass filter for averaging the inductor current, and $G_{ci}(s)$ is the

compensator transfer function. In the voltage loop gain, $G_{vc}(s)$ is the power command control-to-output voltage transfer function, H_v is the output voltage sensing gain, and $G_{cv}(s)$ is the voltage loop compensator transfer function. Each transfer function in the loop gains can be determined based on the power stage dynamics $G_{id}(s)$ and $G_{vc}(s)$. The power stage transfer functions for PFC rectifiers operating in continuous conduction mode are

$$G_{id}(s) = \frac{V_o}{sL} \tag{3.13}$$

$$G_{vc}(s) = \frac{P_{av}}{V_o \cdot V_{control}} \frac{1}{sC} \tag{3.14}$$

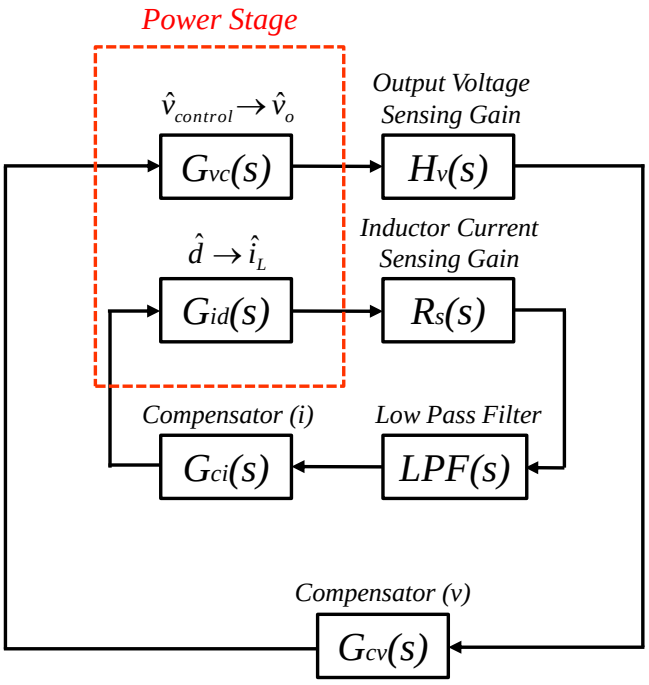


Fig 3.7. Loop Gain Modeling

Since the PFC rectifiers located at the front-end of the power process system of the applications, the power stage dynamics (3.13),(3.14) are developed when the PFC drives the second stage high-bandwidth DC-DC converter. Note that the control-to-output power stage dynamics for both loops are purely capacitive. PI compensators are sufficient for both loops for maintaining the stability margins in terms of bandwidth and phase margin. The loop gains of both loops in CCM are then,

$$\text{Current Loop Gain : } T_i(s) = \frac{V_o}{sL} \cdot R_s \cdot \frac{1}{1 + \frac{s}{\omega_{LPF}}} \cdot G_{ci}(s) \tag{3.15}$$

$$\text{Voltage Loop Gain : } T_v(s) = \frac{P_{av}}{V_o \cdot V_{control}} \cdot \frac{1}{sC} \cdot H_v \cdot G_{cv}(s) \tag{3.16}$$

where ω_{LPF} is the current loop low pass filter cut off frequency, and $V_{control}$ in the voltage loop is the power command fed back to the current reference. Since the compensator design is performed based on the other parameters as shown in (3.15) and (3.16), the tolerances of L and C can modify the each loop gain even with firm compensators. Moreover, in analog control, since the compensator itself is constructed with the combination of passive components, the loop gain uncertainty will be doubled.

3.4 Input Voltage Feedforward

With the average current mode controller in Fig. 3.1, the inner current loop reference i_{ref} can be represented as

$$i_{ref} = H_g \cdot v_g \cdot v_{control} \tag{3.17}$$

where H_g is the input voltage sensing gain, v_g is the input voltage, and $v_{control}$ is the power command. The sensed inductor current i_{sensed} also can be written as

$$i_{sensed} = R_s \cdot \langle i_L \rangle_{T_s} \tag{3.18}$$

Where R_s is the inductor current sensing gain, $\langle i_L \rangle_{T_s}$ represents the average inductor current over a switching period. If it is assumed that the inner current loop works perfectly, the sensed inductor current should track the current loop reference faithfully as

$$R_s \cdot \langle i_L \rangle_{T_s} = H_g \cdot v_g \cdot v_{control} \tag{3.19}$$

In the other hand, the ideal loss free resistor (LFR) model in Fig. 2.3 predicts the average power transferred to the load as

$$P_{av} = \frac{V^2_{g,rms}}{R_e} = P_{load} \tag{3.20}$$

where P_{av} is the average power and P_{load} is the load power. From (3.22), the emulated resistance then can be written as

$$R_e = \frac{v_g}{\langle i_L \rangle_{T_s}} = \frac{R_s}{H_g \cdot v_{control}} \tag{3.21}$$

Finally, the combination of (3.23), (3.24) results in the average power P_{av} expression

$$P_{av} = \frac{V^2_{g,rms} \cdot H_g}{R_s} \cdot v_{control} \tag{3.22}$$

In (3.25), it is shown that when there is an input voltage disturbance, the power command $v_{control}$ is the only variable to be adjusted to maintain the constant average power P_{av} with conventional average current mode controller. However, since $V^2_{g,rms}$

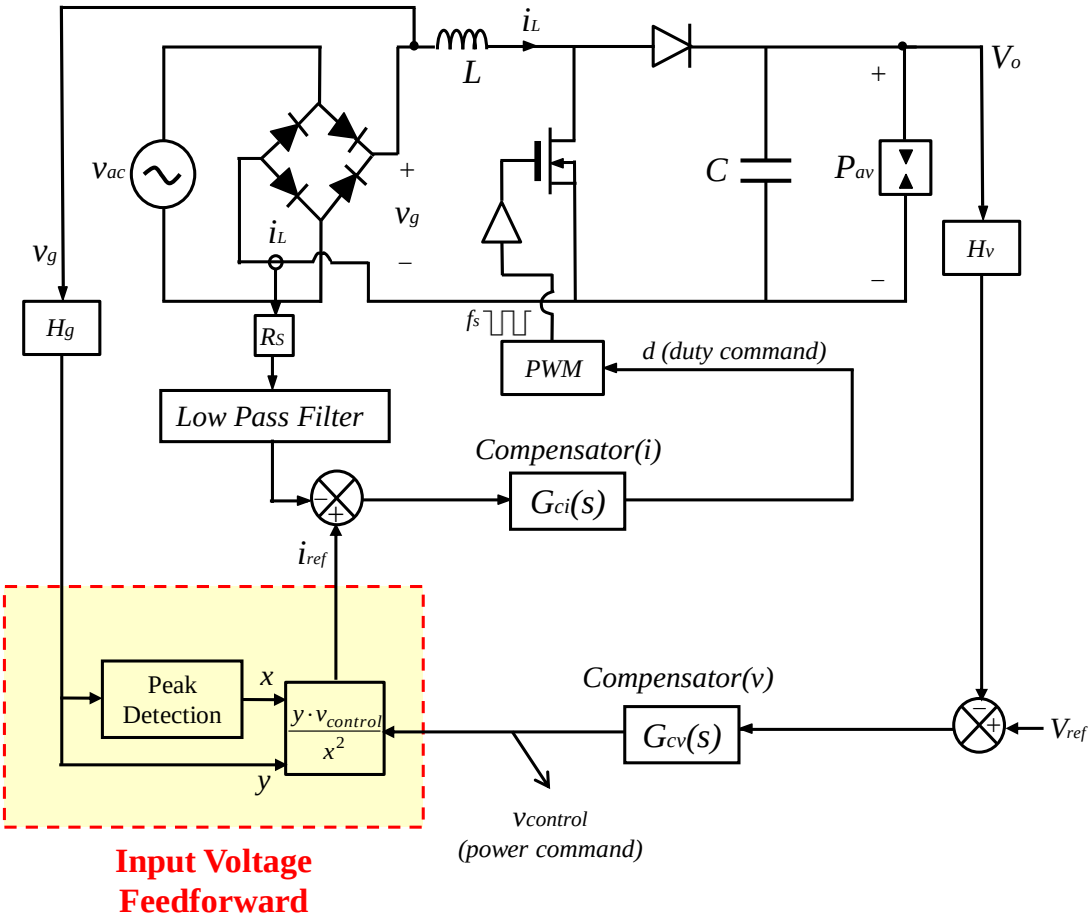


Fig. 3.8. Average current mode controlled PFC rectifier with input voltage feedforward

term is in the nominator, it remains the voltage loop to compensate the input voltage variation, which is not desirable.

This fact calls the need for the input voltage feedforward technique which is shown in Fig. 3.8. The input voltage peak detection circuit and the complex multiplier are implemented to cancel out the input voltage variation effect on the outer voltage loop. In this case, the inner current loop reference i_{ref} becomes

$$i_{ref} = \frac{H_g \cdot v_g \cdot v_{control}}{(H_g \cdot V_M)^2} \tag{3.23}$$

,and the new average power P_{av} expression can be written as

$$P_{av} = \frac{v_{control}}{2 \cdot R_s \cdot H_g} \tag{3.24}$$

From (3.24), it is apparent that the power command $v_{control}$ is only responsible for the average power P_{av} variation, therefore the voltage loop stress is significantly relieved.

The input voltage feedforward also brings dramatic change to the voltage loop gain. From the voltage loop gain in (3.16), the average power P_{av} can be substitute with (3.24), resulting in

$$T_v(s) = \frac{H_v}{2 \cdot H_g \cdot R_s \cdot V_o} \cdot \frac{1}{sC} \cdot G_{cv}(s) \tag{3.25}$$

From (3.25), the voltage loop gain $T_v(s)$ does not affected by the average power P_{av} variation. This characteristic greatly facilitates the loop gain modulation and the passive component values analysis as will be addressed in chapter 5, because the inner current loop gain (3.15), and the outer voltage loop gain (3.25) both shift due to the tolerances of L and C.

CHAPTER 4

Digitally Controlled Boost AC-DC Power Factor Correction (PFC) Rectifiers

In power electronics applications, digital control technique has been drawing much attention for its superb characteristics over analog control in terms of simple implementation, reliable performance against passive components tolerances, and feasibility of advanced control techniques [12]-[23]. With analog control, it is required to implement as many components as needed for desired controller performances, while the digital controller is realized with simple control law equations. This fact significantly simplifies the controller design, and also removes the negative effects of component tolerances on the control loop stability. In addition, the smart control techniques for fast transient response or programmed control law can be implemented with ease, which are infeasible in analog control.

Currently, digital control technique is widely being used in the AC-DC rectifier area. Advanced control techniques such as current programmed control law and wide voltage loop bandwidths are the two mainstream research areas where the digital control is being adopted [13]-[19]. Among them, the digital average current mode control technique, which is one of the most widely used methods, is investigated, and

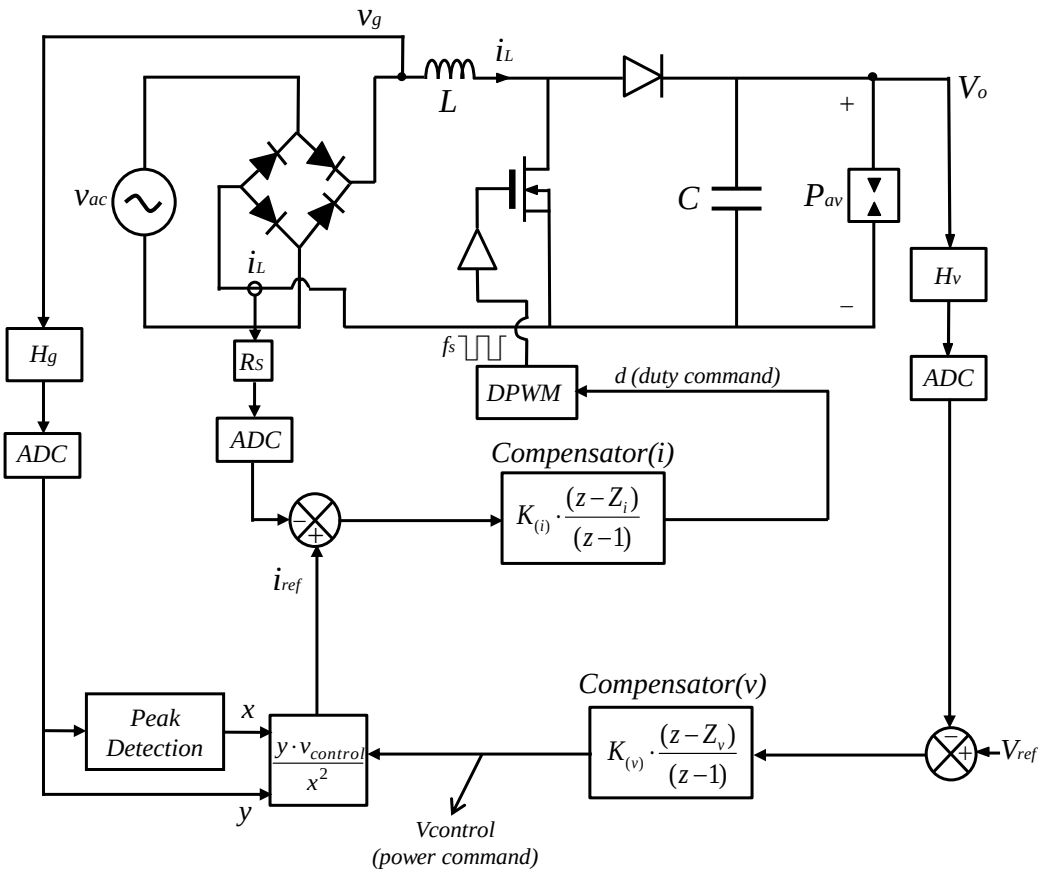


Fig. 4.1. Digital average current mode controlled boost PFC rectifier

implemented on a hardware prototype. The controller design example and corresponding experimental results on the prototype are addressed in the last section of this chapter.

4.1 Digital Average Current Mode Control

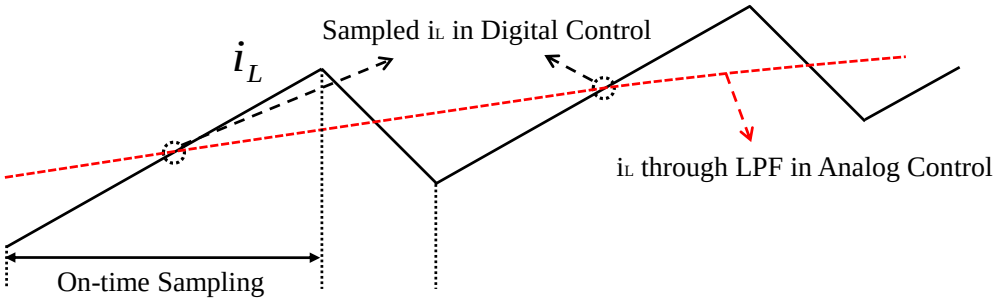
The details of digital average current mode control technique are illustrated in Fig. 4.1. Three analog-to-digital converters (ADC), two discrete-time compensators, and a digital pulse width modulator (DPWM) are implemented instead of analog counterparts. Three ADCs process the informations of the input voltage, input current, and output voltage taken at a specific point of the switching period. The current and voltage loop digital compensators produce the duty command and power command respectively, and the DPWM generates the pulse signal, which drives the switch in the power stage. Detailed sampling actions, timing settings as well as discrete-time design methods are to be addressed.

4.1.1 Rectified Input Voltage (v_g) Sampling

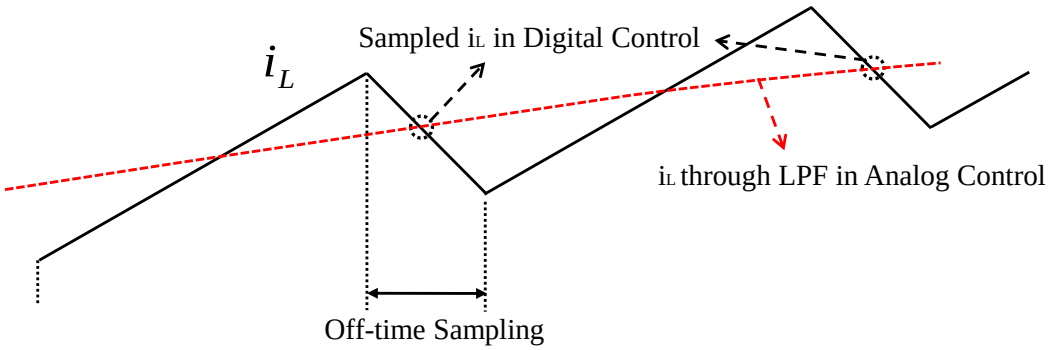
For input current shaping, the rectified input voltage (v_g) has to be fed back as one of the reference components to the current loop. The shape of the sampled rectified input voltage directly becomes the shape of inductor current, which is the rectified version of the input current. Thus, the sampling instance of v_g should be synchronized with the inductor current sampling instance in order to minimize the deviation of the i_L from the shape of actual v_g. In conclusion, v_g sampling occurs exactly at the same time with the inductor current sampling.

4.1.2 Inductor Current (i_L) Sampling

Determining the inductor current sampling instance is the one of the most critical issues in digital averaged current mode control. In analog control, the sensed inductor current go through the low pass filter so that the averaged inductor current tracks the reference as shown in the previous chapter. The same function of the low pass filter in analog control, is assigned to the ADC in digital control. Assuming that the sampling frequency is the same as the switching frequency, sampling values taken from the mid-point of MOSFET switch on-time or off-time represent the whole inductor current during the one switching cycle. Moreover, this mid-point, single sampling per one switching period gives the average inductor current value of each switching cycle [23].



(a) Mid-point on-time sampling



(b) Mid-point off-time sampling

Fig. 4.2. Mid-point switch on-time, off-time sampling of inductor current

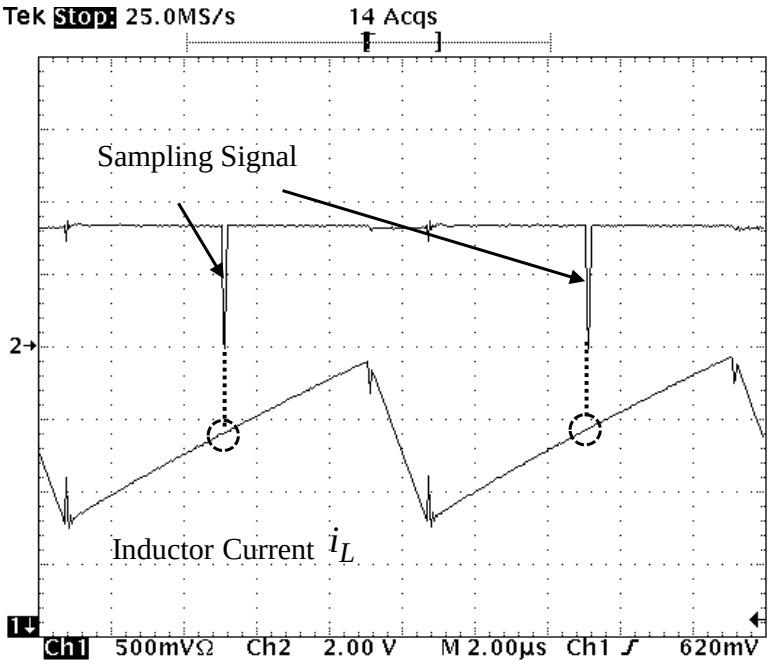


Fig. 4.3. Mid-point, on-time single sampling
ch1: inductor current (i_L) - 500mA/DIV, ch2: Sampling signal – 2V/DIV, Time - 2µs/DIV

As a result, exactly the same function of the analog current loop is done here in a discrete-time manner. In Fig. 4.2, the single, mid-point sampling of each switching cycle is described, and Fig. 4.3 shows real on-time mid-point sampling action on a prototype hardware.

4.1.3 Output Voltage (v_o) Sampling

Generally, the output voltage contains a ripple component which oscillates at twice the line frequency, and the magnitude of ripple depends entirely on the size of bulk output capacitor. In the AC-DC system, from the fact that the input voltage and input current are sinusoidal, it is not difficult to find out that the instantaneous input power is not constant but sinusoidal. The instantaneous input power in PFC rectifier can be defined as

$$p_{ac}(t) = v_g(t) \cdot i_L(t) \tag{4.1}$$

which is the pulsating power. Whereas, in most cases, the PFC rectifier output port is fed with the second stage high-bandwidth DC-DC stage. Thus the output port can be modeled as constant power sink, which equivalently means a constant load power. Then, it is apparent that the instantaneous energy difference between input and output ports has to be compensated from somewhere else. The bulk output capacitor, implemented at the output port, performs this duty, therefore balancing the energy of input and output ports. This is clearly shown in Fig. 4.4. The output bulk capacitor stores the excessive energy when the instantaneous input power exceeds the load power, and supplies the energy to the load when the load power goes below the instantaneous input power. Thus, the ripple on the output capacitor voltage is

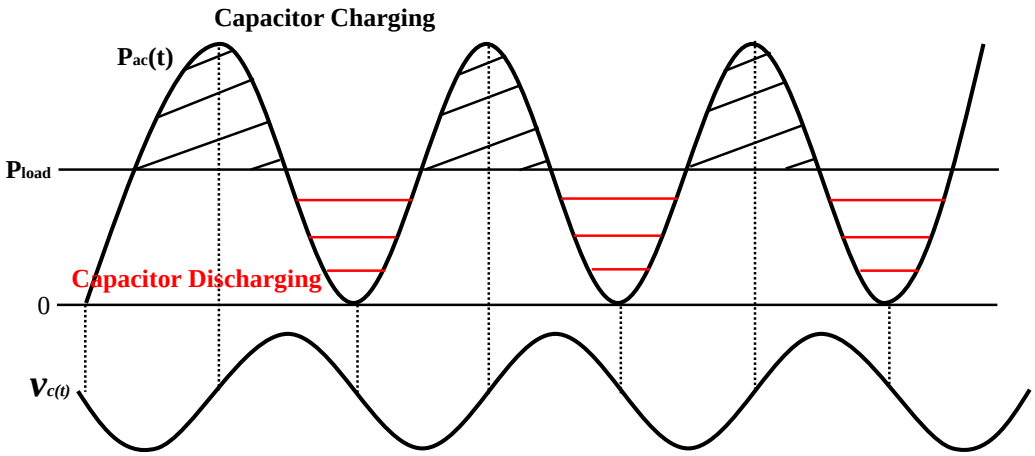
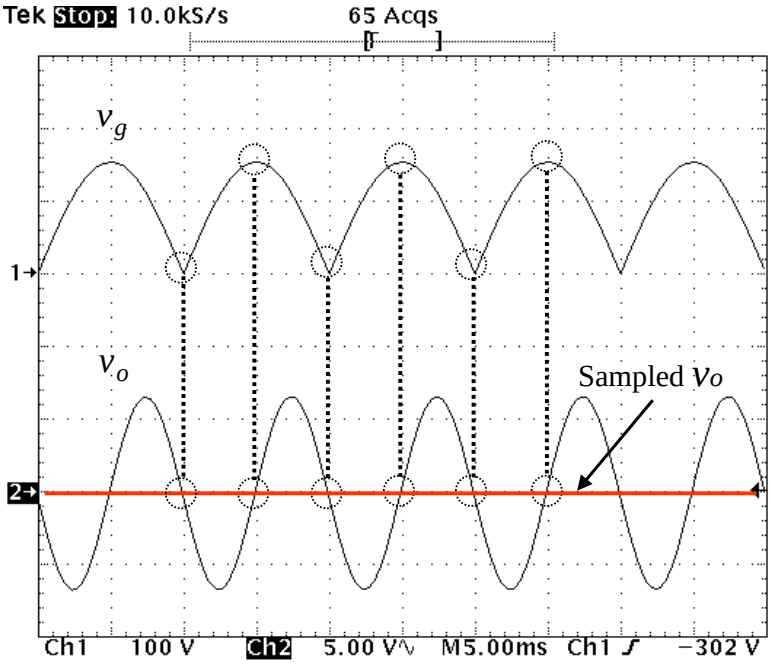
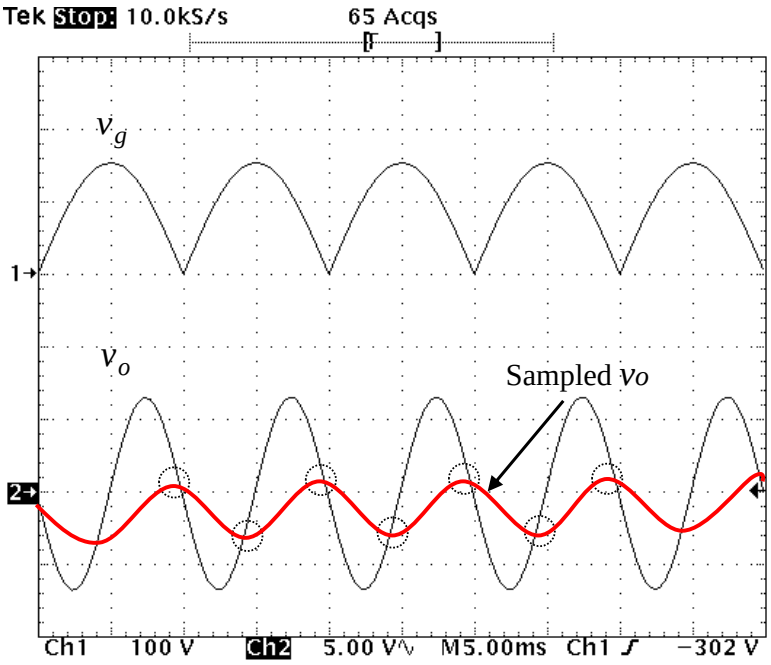


Fig. 4.4. Instantaneous input power, load power, and capacitor voltage

inevitable, and cannot be compensated by the output voltage loop because of low bandwidth. This output voltage ripple, however, can be ignored and filtered when it is fed to voltage loop in digital control. When the sampling instance is synchronized with the rectified input voltage v_g, constant output voltage sampling is possible. Zero crossings and peak points of v_g set the mid-point of output voltage as shown in Fig. 4.5(a). The optimized sampling frequency is therefore four times the line frequency, synchronized with zero and peak points of v_g. Asynchronous sampling signal results in the ripple component superimposed on the sampled values as shown in Fig. 4.5(b).



(a) Synchronous with v_g
Sampling Frequency: $4f_{line}$=200 Hz



(b) Asynchronous sampling
Sampling Frequency: $4f_{line}$=200 Hz

Fig. 4.5. Synchronous sampling vs asynchronous sampling

4.1.4 Digital Compensator

As in analog control, the compensator in digital control can be constructed to perform proportional, integral, and derivative (PID) actions. The only difference is that the digital compensator operates in a discrete-time manner. Only when a trigger signal comes in, the compensator is enabled and produces a new value. The basic compensating law is,

$$G_c(z) = K_P + \frac{K_I}{(1-z^{-1})} + K_D \cdot (1-z^{-1}) \tag{4.2}$$

where K_P is the proportional gain, K_I is the integral gain, and K_D is the derivative gain respectively. This compensating law can be implemented directly, or as a look-up table (LUT) based simplified version.

For AC-DC rectifier, simple digital PI compensators are implemented in both current loop and voltage loop. A detailed compensator signal flow diagram for each loop is shown in Fig. 4.6.

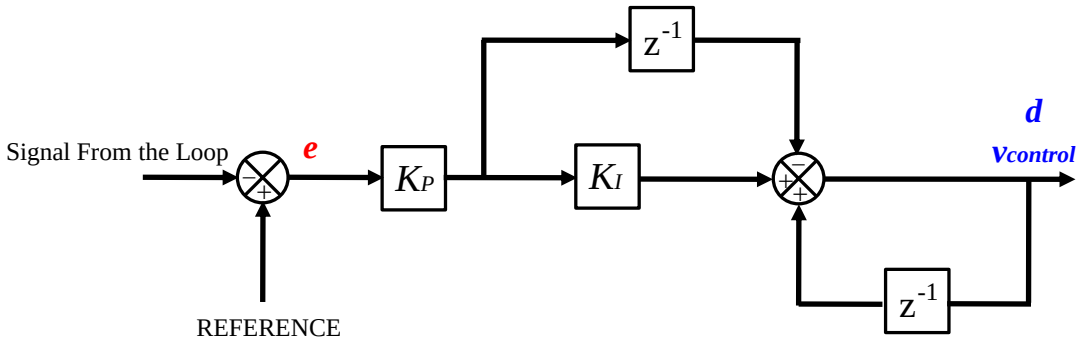
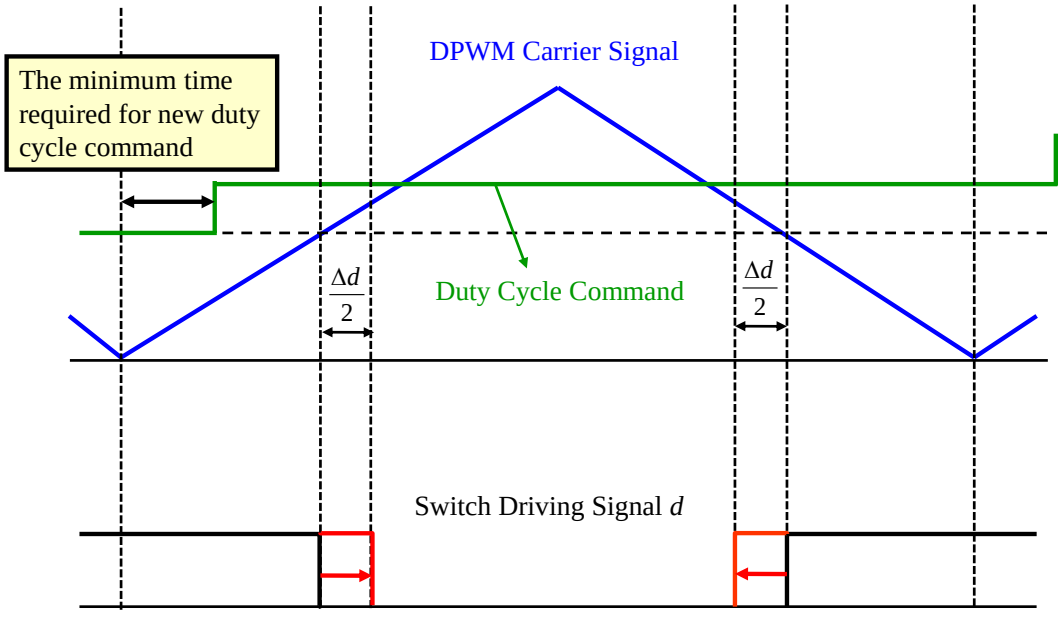


Fig. 4.6. Discrete-time PI compensator block diagram

4.1.5 Digital Pulse Width Modulator (DPWM)

DPWM produces the switch driving signal based on the duty command, which is generated from the current loop compensator. This duty command is compared to the carrier signal generated from the DPWM. Changing duty command results in modulation of switch driving signal at both ends of the saw tooth shape carrier signal as shown in Fig. 4.7. The resolution of DPWM is basically determined by base clock frequency of the control hardware, or can be effectively increased using techniques such as sigma-delta. Fig. 4.7 shows how DPWM processes the input duty command and produces the new switch driving signal.



Fi.g 4.7. Digital pulse width modulator (DPWM)

4.2 Discrete-Time Power Stage Small-Signal Model

Discrete-time power stage transfer function is derived using the method specified in [24,25] and the zero-order-hold method. The discrete-time small-signal response of the duty command (d) to the inductor current (i_L), derived based on the method presented in [24,25] is introduced first and then the discrete-time small-signal response of power command ($v_{control}$) to the output voltage (v_o), derived using the zero-order-hold is addressed later.

4.2.1 $G_{id}(z)$ (the duty command (d) to the inductor current (i_L))

The converter operates in continuous conduction mode, and in each subinterval, the converter is linear, time-invariant. The state space equation for the PFC boost converter in the each switching position is then,

$$\frac{dx(t)}{dt} = Ax(t) + B\begin{bmatrix} V_g \\ V_o \end{bmatrix} \tag{4.3}$$

In this specific case, the input voltage v_g, and the output voltage v_o can be considered as a constant over a switching period. If we let the state x be the inductor current,

$$x(t) = i_L(t) \tag{4.4}$$

The state space equations for each switch state subinterval 1,2, and 3 become

$$L\frac{di_L(t)}{dt} = V_g \tag{4.5}$$

$$L\frac{di_L(t)}{dt} = V_g - V_o \tag{4.6}$$

$$L\frac{di_L(t)}{dt} = V_g \tag{4.7}$$

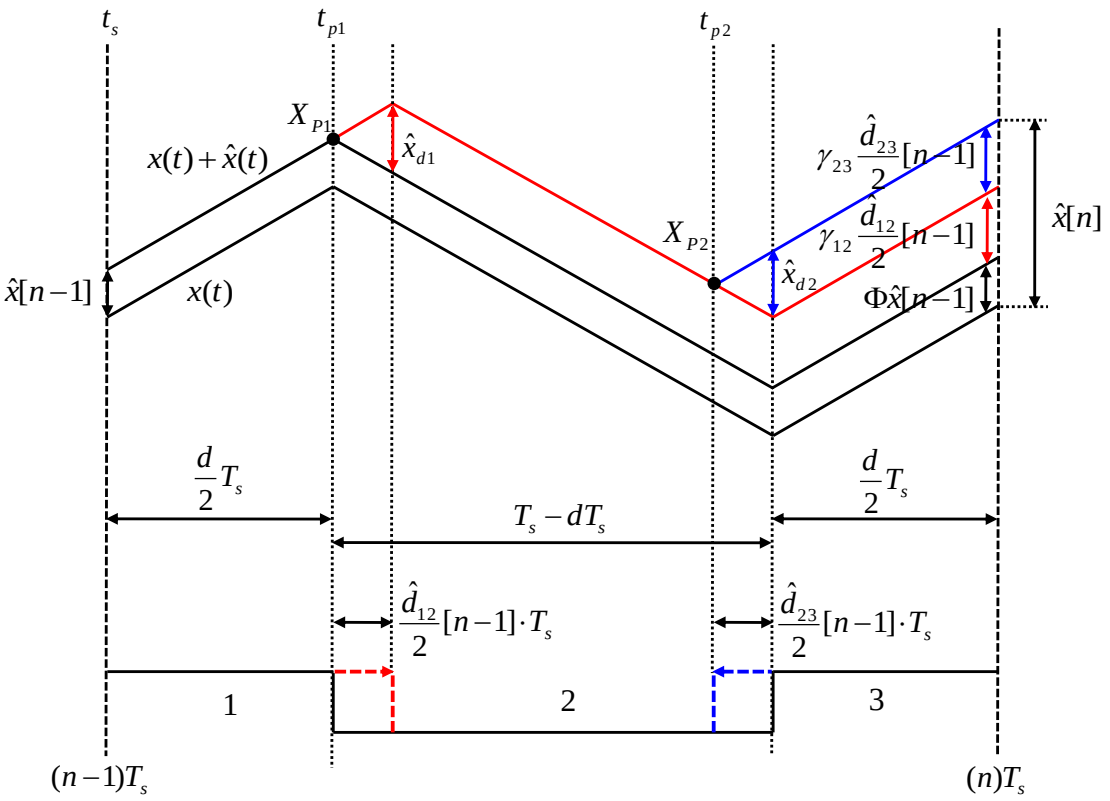


Fig. 4.8. Waveforms illustrated with the effects of small-signal perturbations

The switch states 1,2,3 represent switch on,off, and on time respectively as depicted in Fig. 4.8. Then, the state space representations result in the values of

$$A_1 = 0, \quad B_1 = \begin{bmatrix} \frac{1}{L} & 0 \end{bmatrix} \tag{4.8}$$

$$A_2 = 0, \quad B_2 = \begin{bmatrix} \frac{1}{L} & -\frac{1}{L} \end{bmatrix} \tag{4.9}$$

$$A_3 = 0, \quad B_3 = \begin{bmatrix} \frac{1}{L} & 0 \end{bmatrix} \tag{4.10}$$

In Fig. 4.8, the sampling occurs at t_s, and the modulator samplings are at t_{p1}, and t_{p2}. The Fig. 4.8 illustrates the each perturbation effect, and the final discrete-time small signal model can be expressed as

$$\hat{x}[n] = \Phi\hat{x}[n-1] + \gamma_{12}\frac{\hat{d}_{12}}{2}[n-1] + \gamma_{23}\frac{\hat{d}_{23}}{2}[n-1] \tag{4.11}$$

where the matrices and vector coefficients Φ,$\gamma_{12,}$ and γ_{23} represent the effect of each perturbation term $\hat{x}[n-1]$, $\frac{d_{12}}{2}[n-1]$, and $\frac{d_{34}}{2}[n-1]$ respectively, and will be computed by propagating the effects of these terms. If we consider the effect of $\hat{x}[n-1]$ first, the perturbation propagates through the switch states 1,2, and 3 one by one, and results in the new perturbation $\hat{x}[n]$ after one switching period,

$$\hat{x}[n] = (e^{A_1\frac{d}{2}T_s}\cdot e^{A_2(T_s-dT_s)}\cdot e^{A_3\frac{d}{2}T_s})\cdot\hat{x}[n-1]\Big|_{\frac{\hat{d}_{12}}{2},\frac{\hat{d}_{23}}{2}=0} \tag{4.12}$$

,which means

$$\Phi = e^{A_1\frac{d}{2}T_s}\cdot e^{A_2(T_s-dT_s)}\cdot e^{A_3\frac{d}{2}T_s} = 1 \tag{4.13}$$

The effect of $\frac{d_{12}}{2}[n-1]$ propagates the switch states 2, 3, and causes the perturbation of $\hat{x}_{d1}$ at the end point of subinterval 1. $\hat{x}_{d1}$ can be represented as

$$\hat{x}_{d1} = (A_1X_{P1} + B_1\begin{bmatrix}V_g\\V_o\end{bmatrix})\frac{\hat{d}_{12}}{2}T_s - (A_2X_{P1} + B_2\begin{bmatrix}V_g\\V_o\end{bmatrix})\frac{\hat{d}_{12}}{2}T_s \tag{4.14}$$

Finally, the coefficient γ_{12} becomes

$$\gamma_{12} = e^{A_2(T_s-dT_s)}\cdot e^{A_3\frac{d}{2}T_s}\cdot\alpha_{12}T_s = \alpha_{12}T_s \tag{4.15}$$

where

$$\begin{aligned}\alpha_{12} &= (A_1 X_{P1} + B_1 \begin{bmatrix} V_g \\ V_o \end{bmatrix}) - (A_2 X_{P1} + B_2 \begin{bmatrix} V_g \\ V_o \end{bmatrix}) \\ &= (B_1 - B_2) \begin{bmatrix} V_g \\ V_o \end{bmatrix} = \begin{bmatrix} 0 & \frac{1}{L} \end{bmatrix} \begin{bmatrix} V_g \\ V_o \end{bmatrix} = \frac{V_o}{L}\end{aligned} \tag{4.16}$$

In the case of $\frac{d_{12}}{2}[n-1]$ perturbation effect, it goes through the switch state 3 only, and the resulting perturbation can be written as

$$\hat{x}_{d2} = (A_3 X_{P2} + B_3 \begin{bmatrix} V_g \\ V_o \end{bmatrix}) \frac{\hat{d}_{23}}{2} T_s - (A_2 X_{P1} + B_2 \begin{bmatrix} V_g \\ V_o \end{bmatrix}) \frac{\hat{d}_{23}}{2} T_s \tag{4.17}$$

Then, the coefficient γ_{23} is,

$$\gamma_{23} = e^{A\frac{d}{2}T_s} \alpha_{23} T_s = \alpha_{23} T_s \tag{4.18}$$

where

$$\begin{aligned}\alpha_{23} &= (A_3 X_{P2} + B_3 \begin{bmatrix} V_g \\ V_o \end{bmatrix}) - (A_2 X_{P2} + B_2 \begin{bmatrix} V_g \\ V_o \end{bmatrix}) \\ &= (B_3 - B_2) \begin{bmatrix} V_g \\ V_o \end{bmatrix} = \begin{bmatrix} 0 & \frac{1}{L} \end{bmatrix} \begin{bmatrix} V_g \\ V_o \end{bmatrix} = \frac{V_o}{L}\end{aligned} \tag{4.19}$$

X_{P1},and X_{P2} are the vector of steady-state variables at the points specified in the Fig. 4.8 respectively. Since the values of A_1,A_2, and A_3 are all zeros, and $\hat{d}_{12} = \hat{d}_{23}$, the final discrete-time small signal model becomes

$$\begin{aligned}\hat{x}[n] &= \hat{x}[n-1] + \frac{V_o \cdot T_s}{L} \frac{\hat{d}}{2}[n-1] + \frac{V_o \cdot T_s}{L} \frac{\hat{d}}{2}[n-1] \\ &= \hat{x}[n-1] + \frac{V_o \cdot T_s}{L} \hat{d}[n-1]\end{aligned} \tag{4.20}$$

Finally, standard z-transform of (3.20) yield the control-to-inductor current transfer function of

$$G_{id}(z) = \frac{\hat{i}_L}{\hat{d}} = \frac{V_o \cdot T_s}{L} \frac{1}{z-1} \tag{4.21}$$

4.2.2 $G_{vc}(z)$ (the power command ($v_{control}$) to the output voltage (v_o))

The voltage loop power stage discrete-time small-signal modeling is conducted using the zero-order hold method based on the continuous-domain model [26]. In the voltage loop, only sample-and-hold delay effect is introduced, and all the other computation delays are ignored since sampling period is long enough. The continuous time plant transfer function is followed by sampling and zero-order-hold block as shown in Fig. 4.9. The continuous time power stage model, which is derived in the previous chapter can be written as

$$G_{vc}(s) = \frac{H_v}{2 \cdot H_g \cdot R_s \cdot V_o} \cdot \frac{1}{sC} \tag{4.22}$$

Thus, the zero-order hold with the sampling rate of 4 times a line frequency, becomes

$$\begin{aligned} G_{vc}(z) &= Z\left[G_{vc}(s) \cdot \frac{1-e^{-sT_{sampling}}}{s} \right] \\ &= Z\left[\frac{H_v}{2 \cdot R_s \cdot H_g \cdot V_o \cdot C} \cdot \frac{1-e^{-sT_{sampling}}}{s^2} \right] \\ &= (1-z^{-1}) \cdot \frac{H_v}{2 \cdot R_s \cdot H_g \cdot V_o \cdot C} \cdot Z\left[\frac{1}{s^2} \right] \\ &= \frac{H_v}{2 \cdot R_s \cdot H_g \cdot V_o \cdot C} \cdot \frac{T_{sampling}}{z-1} \end{aligned} \tag{4.23}$$

Finally, the discrete-time domain small-signal transfer function can be computed using (3.23), resulting in

$$G_{vc}(z) = \frac{H_v}{2 \cdot R_s \cdot H_g \cdot V_o \cdot C} \cdot \frac{T_{line}}{4} \frac{1}{z-1} \tag{4.24}$$

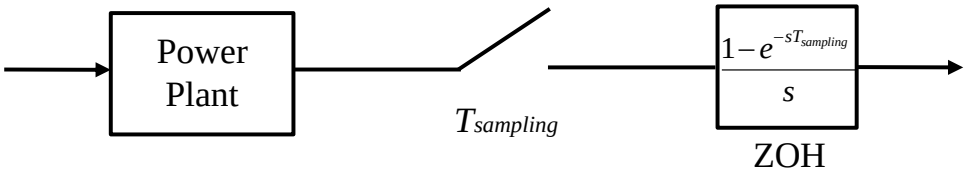


Fig. 4.9. Sample and hold block diagram

4.3 Control Loops Design Example

The control loops are designed based on the the boost PFC rectifier prototype built with the following parameters: $V_{g,rms}$=110 V_{rms} or 230 V_{rms} , f_{line}= 50 Hz, V_o=380 V, f_s=100 kHz, L=0.5 mH, C=220 μF, P_{av}=300 W ~ 500 W. The digital controller was HDL coded and implemented on a Xilinx Virtex-IV FPGA. 8bit ADCs, Digital PI compensators, and the 10-bit DPWM are adopted. Based on the digital average current mode control technique, each control loop component parameter and timing are set in detail for desired stability margins in terms of control loop bandwidths, phase margins. As addressed, the current loop requires high bandwidth, and the voltage loop needs less than 10Hz of bandwidth. The loop gain expression for each loop is

$$\text{Current Loop Gain}: \ T_i(z) = G_{id}(z) \cdot G_{ci}(z) \cdot G_{DPWM}(z) \cdot R_s \qquad (4.25)$$

$$\text{Voltage Loop Gain}: \ T_v(z) = G_{vc}(z) \cdot G_{cv}(z) \cdot H_v \qquad (4.26)$$

In the current loop gain, $G_{id}(z)$ is the control-to-inductor current transfer function, $G_{ci}(z)$ is the current loop compensator, $G_{DPWM}(z)$ is the DPWM transfer function, and R_s is the current sensing gain. In the voltage loop gain, $G_{vc}(z)$ represents the control-to-

output voltage transfer function, $G_{cv}(z)$ is the voltage loop compensator, and H_v is the output voltage sensing gain. If the current loop is designed first, based on the power stage control-to-inductor current transfer function obtained from the discrete-time small signal modeling, which is

$$G_{id}(z) = 7.6 \cdot \frac{1}{z-1} \tag{4.27}$$

, the compensator can be designed in such a way that the current loop gain obtains the specific bandwidth and phase margin. If the duty cycle command is correctly scaled, then the DPWM transfer function $G_{DPWM}(z)$ is simply the height of carrier signal, which is typically equal to 1. The sensing gain is determined by the designer, and it is assumed as 1 in this case. Then, the compensator design such that the loop gain has 10kHz bandwidth and 55° phase margin is,

$$G_{ci}(z) = 0.0702 + \frac{0.0156}{(1-z^{-1})} \tag{4.28}$$

This PI compensator adds integral action and one zero. The current loop gain bode plot in Fig. 4.10 shows the desired stability margins. The voltage loop is designed so that it has 5Hz bandwidth and 68° phase margin. The sensing gain H_v is 1, and the power stage transfer function is,

$$G_{vc}(z) = 6.57 \cdot \frac{1}{z-1} \tag{4.29}$$

Then, the compensator design to meet the voltage loop stability margins is

$$G_{cv}(z) = 0.0753 + \frac{0.0051}{1-z^{-1}} \tag{4.30}$$

The bode plots in Fig. 4.10 and 4.11 verify that the design requirements have been achieved. Both current and voltage control loops are designed for the desired stability

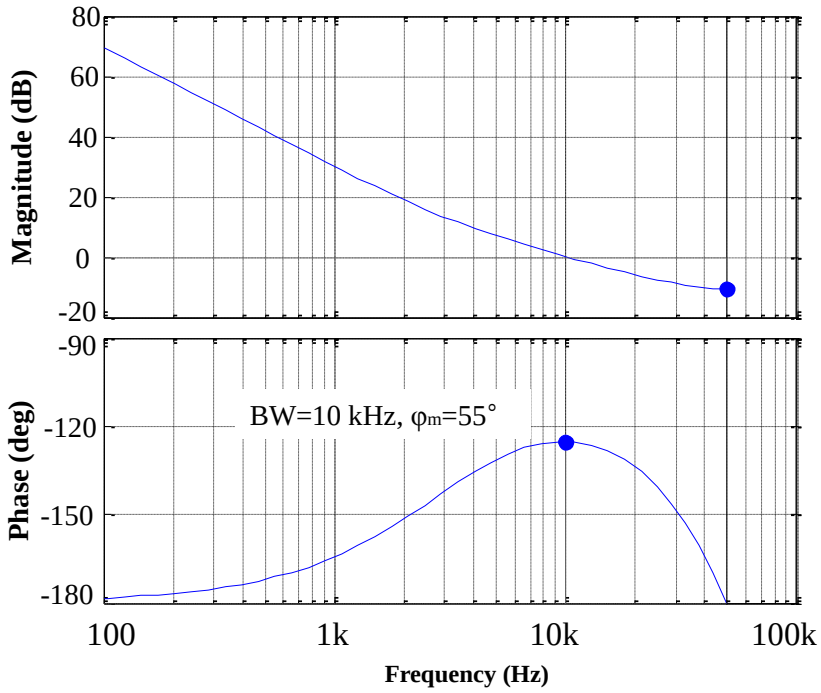


Fig. 4.10. The current loop gain bode diagram

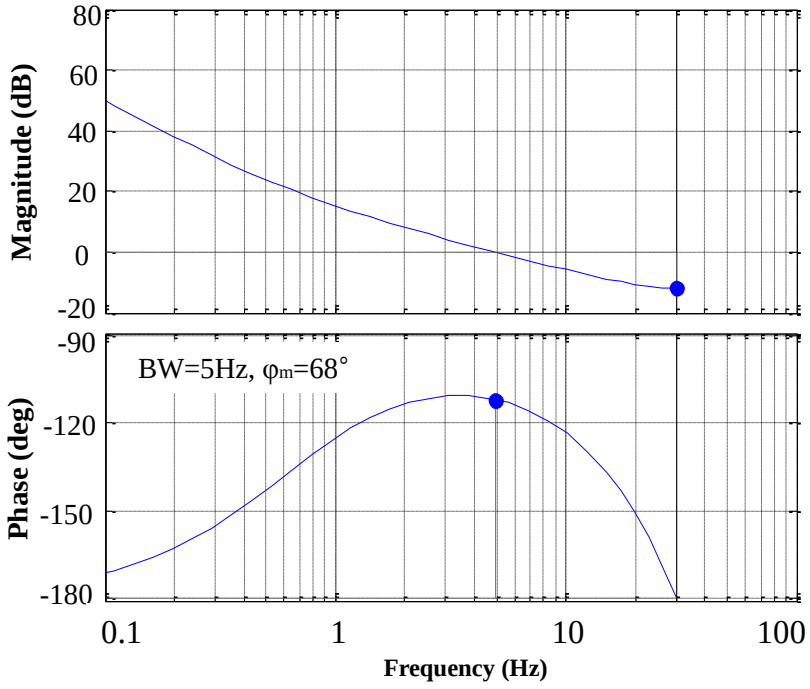


Fig. 4.11. The voltage loop gain bode diagram

margins. In digital control, the timing setting of the signal processing is also as important as the control parameter designs. Especially, the current loop signal flow should be set carefully such that the new duty ratio produced from the controller should be ready quickly enough to be applied to the corresponding switching period where the inductor current and rectified voltage information is acquired. Since the inductor current and rectified input voltage change every switching cycle, it is important to compute and apply the new duty cycle value to the switch as quickly as possible. In Fig. 4.12, the delay time from the power stage information latch instance to the new duty cycle instance is specified in detail.

7822BRZ 8-bit ADCs are used for the power stage information analog-to-digital conversions , which has 420ns maximum conversion time from the sample instance to the output produce. 50ns is inserted before the compensator computation starting point to guarantee that the power stage information is ready for computation.

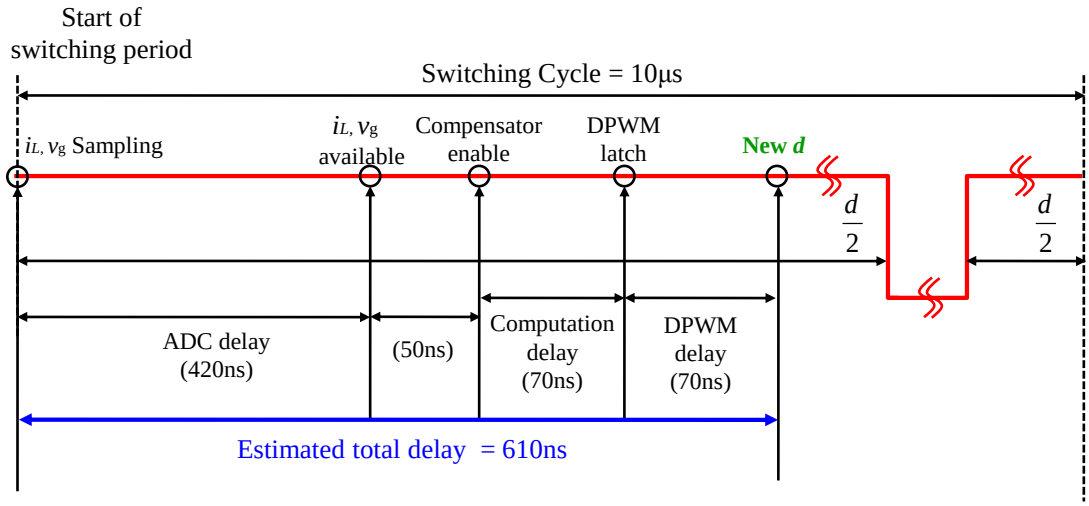


Fig. 4.12. Digital controller timing setting

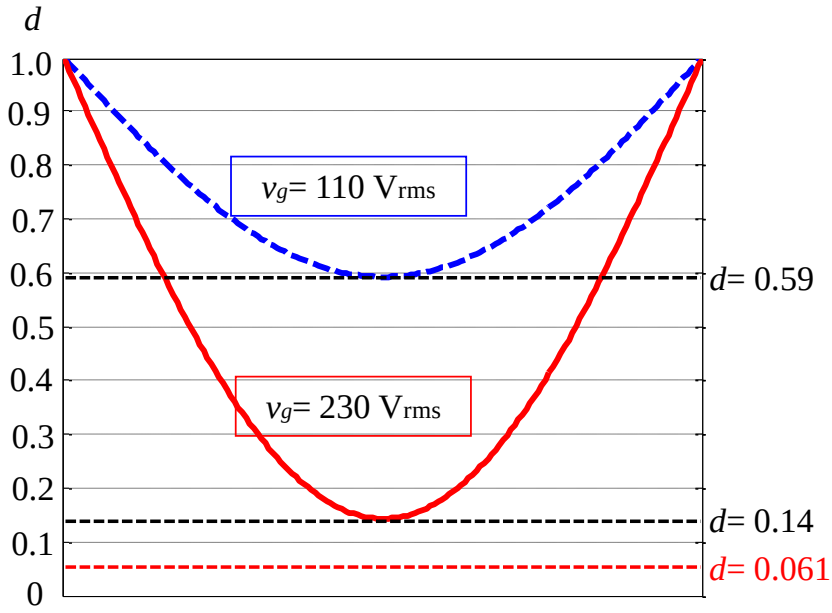
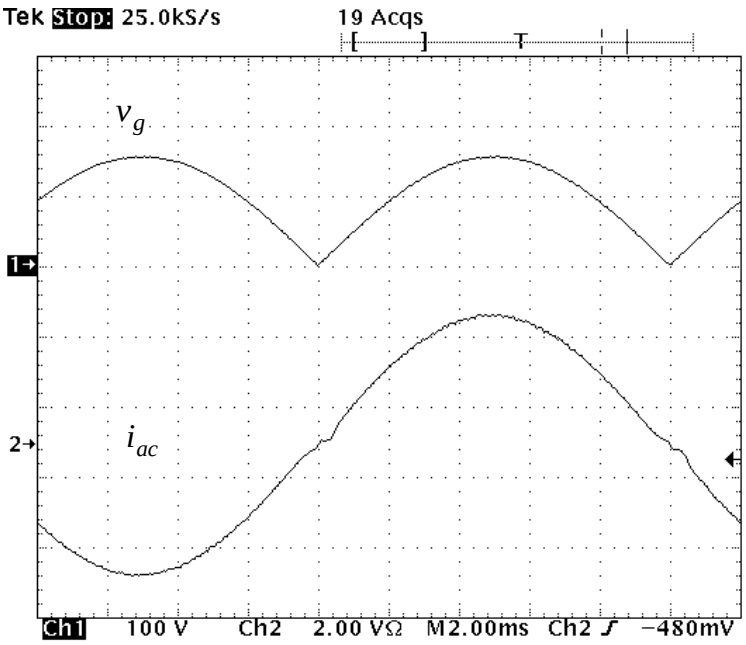


Fig. 4.13. Nominal duty cycle command for the universal input voltages 110 V_{rms}, 230 V_{rms}

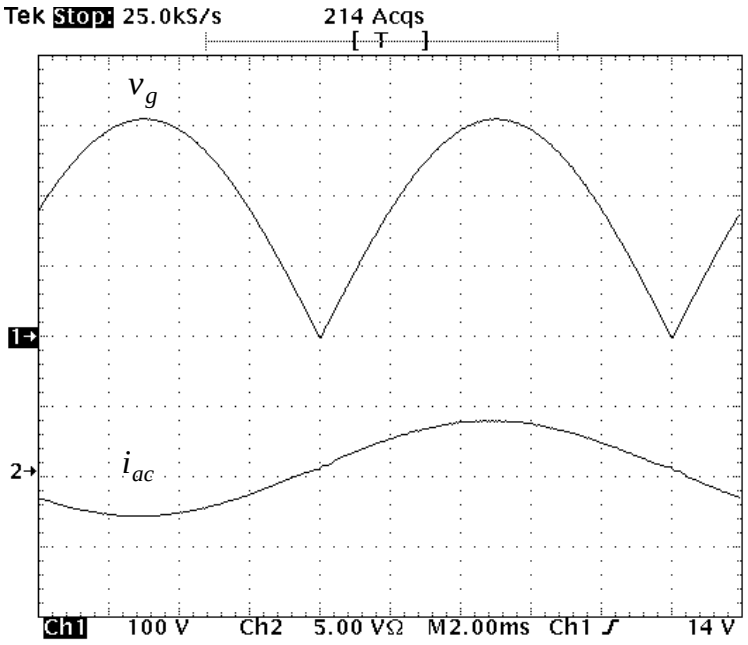
70ns is assigned to the compensator for new duty command computation. Finally, the estimated total time for new duty command generation is therefore approximately 610 ns. This estimated total time is 6.1% of total switching period, which is 10 μs. That means that the DPWM is not able to produce the duty cycle less than 6.1%, because it is the minimum time required for new duty cycle generation. Thus, the FPGA controller is implemented to maintain at least 6.1% of duty command. From the duty cycle computed using the equation (1.11) developed in Chapter 1, the minimum duty command for the universal input ranges 110 V_{rms}~230 V_{rms}, does not go below 6.1%, and it works for the suggested timing setting. In Fig 3.12, we can observe that 110 V_{rms} and 230 V_{rms} input voltages result in the minimum duty cycle ratio of 59% and 14% respectively, higher than 6.1%.

4.4 Exprimental Results

Experimental results show the performance of boost PFC rectifier with the parameters specified in the controller design section. Current shaping operation, the output voltage regulation ability are confirmed for the input voltage of 110 V_{rms}~220 V_{rms} and 50 Hz frequency in Fig. 4.14.



(a) $v_{g,rms}$=110 V_{rms}, f_{line}= 50 Hz
ch1: Input current(i_{ac})-2A/Div, and ch2: Rectified input voltage(v_g)-100V/Div time-2*ms*/Div



(b) $v_{g,rms}$=220 V_{rms}, f_{line}= 50 Hz
ch1: Input current(i_{ac})-2A/Div, and ch2: Rectified input voltage(v_g)-100V/Div time-5*ms*/Div

Fig. 4.14. Normal system operation for wide input voltage range

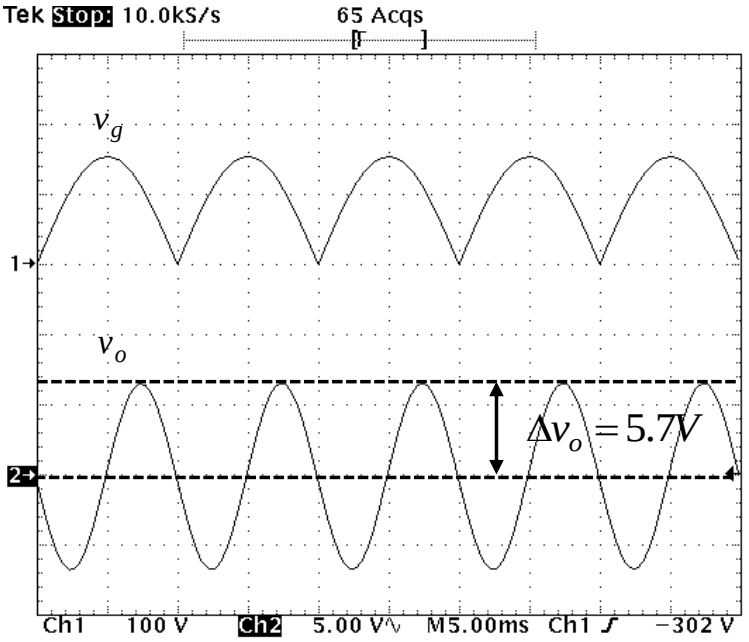


Fig. 4.15. Output voltage regulation ch1:Rectified input voltage(v_g)-100V/Div and ch2:ac coupled output voltage (V_o)-5V/Div, time-5*ms*/Div, f_s=50 Hz

Output voltage ripple magnitude can be calculated from the equation

$$\Delta V_o = \frac{P_{load}}{2 \cdot \omega_{line} \cdot V_{o,rms} \cdot C} \tag{4.31}$$

P_{load} is the output power, ω_{line} is the line frequency, and $V_{o,rms}$ is the output voltage, C is the output bulk capacitance. The ripples are calculated as 5.7 V for 50 Hz. The experimental results are verified in Fig 4.15.

CHAPTER 5

Auto-tuning of Digitally Controlled Boost AC-DC Power Factor Correction (PFC) Rectifiers

In power electronics applications, digital control techniques have been explored to achieve design and performance advantages such as programmability, improved dynamic responses, or improved robustness, offered by the abilities to practically implement more advanced control techniques [12].

In the area of low harmonic PFC rectifiers, various digital control techniques have been introduced to achieve high-performance power-factor correction, low current harmonics, improved efficiency, or improved voltage-loop dynamic responses [13]-[19]. Previously described digital control techniques for PFC rectifiers are still vulnerable to tolerances in the power stage components, which may result in degraded system performance in terms of stability margins, harmonics, or dynamic responses. With component uncertainties or tolerances, power plant dynamics may be substantially different compared to the nominal conditions assumed in the design of the current-loop and the voltage-loop compensators.

Recently, a number of on-line identification methods and auto-tuning techniques, which can achieve more robust and reliable performances of feedback

loops have been proposed in the dc-dc area [27]-[32]. Among them, auto-tuning techniques based on the perturbation signal injection into the feedback control loop are proposed in [29]-[31]. In a digitally controlled dc-dc converter, a tuner perturbs the voltage feedback loop and measures the response of the system. Compensator parameters are then adjusted to respond to variations of the power plant parameters or operating conditions.

This chapter extends this auto-tuning approach to digitally controlled boost PFC rectifiers as illustrated in Fig. 5.1. Based on the digital average current mode

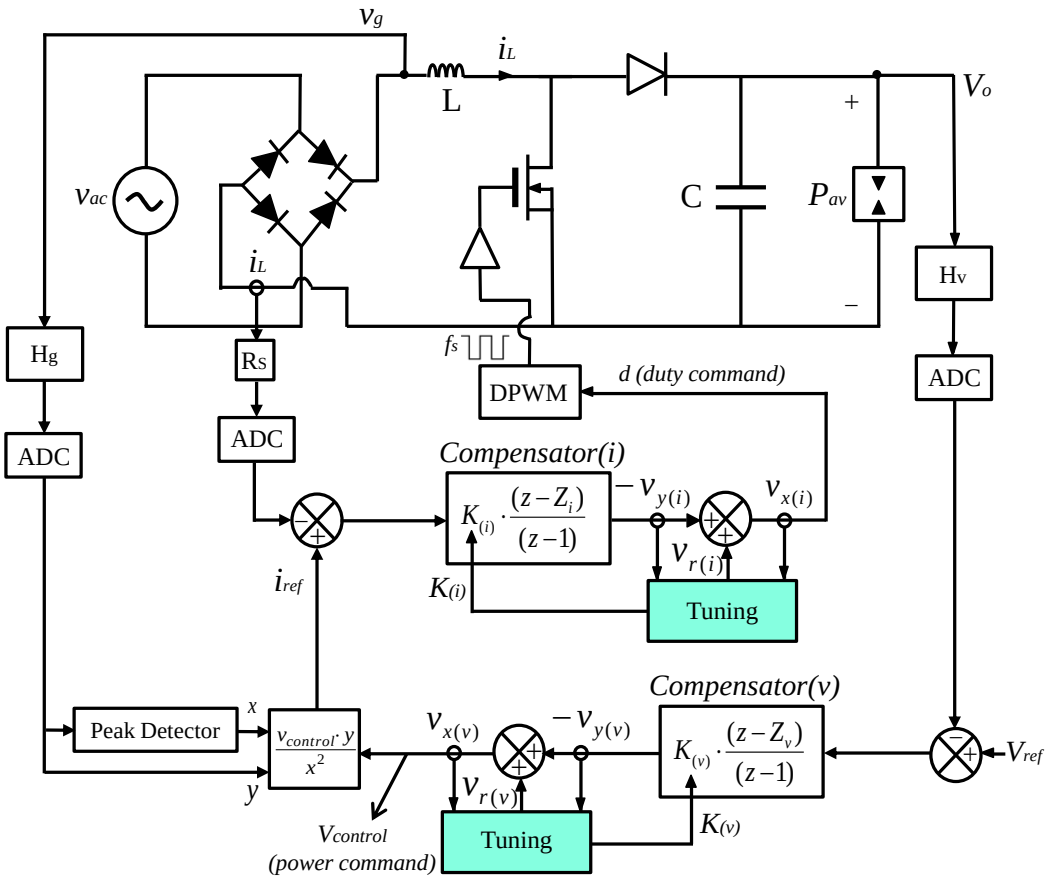


Fig. 5.1. Digital averaged current mode controlled boost power factor correction (PFC) rectifier with proposed auto-tuning

control technique, tuners are implemented in both current and voltage loops to inject the perturbations and analyze the loop responses at the injection frequencies. As will be explained in the following sections, a tuning module is realized using simple arithmetic computations.

As a side benefit, the proposed approach enables real-time estimation of the power-stage inductance L and capacitance C values, facilitating accurate CCM/DCM boundary detection and current waveform prediction as further potentials. Since this approach is based on the perturbation injection method, tuning can be activated at start-up or on command to avoid any undesirable effects of the perturbation signal in normal operation.

This chapter is organized as follows. In Section 5.2, loop gain characteristics of the current and the voltage loops in a boost PFC rectifier are discussed. Analysis and realization of the proposed auto-tuning approach are presented in Section 5.3, while experimental results are given in Section 5.4. Section 5.5 concludes the chapter

5.1. Tolerances of L and C

Even if the precise inductance and capacitance values are computed and chosen according to the design constraints, the real passive components values are not precise due to tolerances. This will worsen as temperature increases or the system ages. Typical inductor tolerance lies between ±20%~±40% depending on the core choices, and this inductance tolerance causes the deviation of the current loop gain from the nominal operating point. Furthermore, it degrades the performance of the digital current-programmed control techniques, since they are developed based on the

nominal inductance value. Tight inductance tolerance is essential in current loop control of AC-DC PFC rectifiers. Capacitors, especially aluminum electrolytic capacitors, typically have ±20% tolerances and worsen with age. As it approaches the end of its lifetime, the tolerance can surge up to more than ±50% of the nominal value. The tolerance deteriorates as temperature goes up, and the high temperature, again shorten the lifetime of the capacitor, thus aggravating the situation furthermore. The capacitor tolerance is the counterpart of the inductor tolerance in the voltage loop. These unexpected filer component values modify the loop gains and stability margins as addressed. However, while the system is operating, the only possible on-line estimation method of these tolerances is guessing by referring to the datasheets. It is obvious that the acquisition of accurate L and C values guarantees the whole control system stability margins maintenance. Regardless of other design constraints such as efficiency, if the controller is capable of maintaining the stability margins against uncertain filter component value variations, tight tolerance is no longer needed. As will be discussed in the later sections, these unpredictable component tolerances can be compensated in a control point of view by adopting a proposed advanced control technique, therefore widening the choice of components irrespective of tolerance constraints.

5.2. Loop Gain Characteristics of the AC-DC Boost Power Factor Correction Rectifier

When a boost PFC rectifier drives a high bandwidth dc-dc stage – modeled as a power sink in Fig. 5.1 – continuous-time expressions for the current and voltage loop gains $T_i(s)$ and $T_v(s)$ are found to be [6]:

$$T_i(s) = G_{ci}(s) \cdot \frac{V_o}{sL} \tag{5.1}$$

$$\begin{aligned} T_v(s) &= G_{cv}(s) \cdot \frac{P_{av}}{V_o \cdot V_{control}} \cdot \frac{1}{sC} \cdot H_v \\ &= G_{cv}(s) \cdot \frac{1}{2 \cdot V_o \cdot R_s \cdot H_g} \cdot \frac{1}{sC} \cdot H_v \end{aligned} \tag{5.2}$$

where $G_{ci}(s)$ and $G_{cv}(s)$ are the transfer functions of the current and voltage loop compensators, respectively, P_{av} is the output power, $V_{control}$ is the power command, V_o is the output voltage, and H_v is the output voltage sensing gain. R_s and H_g represent the inductor current and rectified input voltage sensing gains respectively.

In the current loop gain (5.1), all the parameters in the loop gain expression are known with the exception of L, the value of which may be subject to uncertainties or tolerances. Similarly, in the case of the voltage loop, if the rectified input voltage feedforward is applied, the only parameter subject to uncertainties or tolerances in the voltage loop gain (5.2) is the capacitance C. Furthermore, the phase responses of the uncompensated loop gains do not depend on L or C. This means that the phase compensation does not require tuning and can be carried out through proportional-integral (PI) compensators having fixed zero locations.

On the other hand, the magnitude responses of T_i and T_v scale according to the parameter variations of L and C, respectively, as sketched in Fig. 5.2. The dotted lines represent the loop gain magnitude response shifted up or down due to parameter tolerances. As a result, the corresponding crossover frequency shifts from a nominal value to f_{cmax} or f_{cmin} respectively. From the foregoing considerations, both desired crossover frequency and phase margin can be achieved by simply adjusting the compensator gain, because phase margin will automatically reach the desired value as the gain is adjusted to obtain the target crossover frequency. Therefore, only the gain of the compensator needs to be tuned to achieve the target phase margin and crossover frequency. This simplifies the tuner, allowing a hardware-effective implementation suitable for low-cost PFC controller applications.

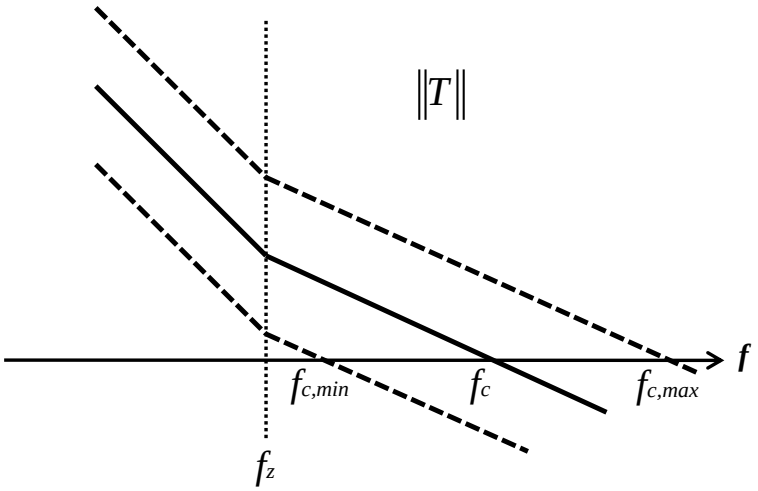


Fig. 5.2. Loop gain with PI compensator at nominal operating condition (**solid line**), and deviated loop gains due to component (L or C) tolerances (**dashed lines**)

It is also apparent that the tolerances of L and C can be indirectly estimated from the modified compensator gains, as the degree of the loop gain deviation from the nominal operating point corresponds to the tolerances of L and C

5.3 Tuning Controller

Two digital auto-tuners are employed for tuning the current and voltage loop gains respectively, as shown in Fig. 5.1. Each tuner injects a digitally generated sinusoidal perturbation v_r, oscillating at the desired crossover frequency f_c, into the corresponding loop, and monitors signals v_x and v_y before and after the injection point in order to estimate the loop gain magnitude deviation from unity. The signals v_r, v_x and v_y can be represented as

$$v_r = \| v_r \| \cdot \sin \omega_c t \tag{5.3}$$

$$v_x = v_{x,inj} + v_{x,other} \tag{5.4}$$

$$v_y = v_{y,inj} + v_{y,other} \tag{5.5}$$

where $v_{y,inj}$ and $v_{x,inj}$ represent the injected frequency components in the signals v_x and v_y respectively, and $v_{x,other}$, $v_{y,other}$ are the remaining frequency components (other than the injected frequency) in v_x and v_y respectively. Through simple corrections of the current and voltage compensator gains $K_{(i)}$ and $K_{(v)}$, both the desired control bandwidth and phase margin can be obtained.

A digitally generated sinusoidal perturbation v_r, oscillating at the desired crossover frequency f_c, is injected into the loop; the loop-gain at $f = f_c$ is [33]:

$$T = \frac{v_{y,inj}}{v_{x,inj}} \tag{5.6}$$

The same approach to on-line loop-gain measurement has been applied in [29]-[32]. The tuning objective is to achieve unity loop gain at $f = f_c$, i.e. to equalize the amplitudes of signals $v_{x,inj}$ and $v_{y,inj}$:

$$\|T(\omega_c)\| = 1 \tag{5.7}$$

In order to achieve (5.7), the tuner processes signals v_x and v_y to derive a tuning error, i.e. a measure of how far the system is from (5.7). The tuning error is then accumulated via an integrator. The integrator output acts on the compensator gain in order to null the tuning error and therefore realize (5.7).

5.3.1 Tuning Objective and signal orthogonality

Equivalence between the tuning objective (5.7) and signal orthogonality is shown in this section. If the closed loop system is considered a linear system for small-signal perturbations, then signals $v_{x,inj}$ and $v_{y,inj}$ only contain the perturbation frequency f_c. As will be now derived, this fact implies a specific relationship between signals $v_{x,inj}$, $v_{y,inj}$ and v_r; in the frequency domain, these signals can be written as

$$V_r(\omega) = \vec{v}_{rm} \cdot \delta(\omega - \omega_c) + \vec{v}_{rm}{}^* \cdot \delta(\omega + \omega_c) \tag{5.8}$$

$$V_{x,inj}(\omega) = \frac{V_r(\omega)}{1 + T(\omega)} \tag{5.9}$$

$$V_{y,inj}(\omega) = \frac{T(\omega)}{1 + T(\omega)} \cdot V_r(\omega) \tag{5.10}$$

where $\vec{v}_{rm}$ represents the phasor of perturbation (5.3). Subtraction of (5.10) from (5.9) yields

$$V_{x,inj}(\omega) - V_{y,inj}(\omega) = \frac{1-T(\omega)}{1+T(\omega)} \cdot V_r(\omega) \tag{5.11}$$

Consider now the inner product of the signals v_x-v_y and the perturbation v_r :

$$\begin{aligned} \left\langle v_x(t) - v_y(t), v_r(t) \right\rangle &= \int_{-\infty}^{\infty} (v_x(\tau) - v_y(\tau)) \cdot v_r(\tau) d\tau \\ &= \int_{-\infty}^{\infty} (V_x(\omega) - V_y(\omega)) \cdot V_r^*(\omega) d\omega \end{aligned} \tag{5.12}$$

Given that the V_r term in the right-hand side of (5.12) only contains the injection frequency component, and considering (5.8) and (5.11), the inner product calculation can be further developed as:

$$\begin{aligned} &\int_{-\infty}^{\infty} (V_x(\omega) - V_y(\omega)) \cdot V_r^*(\omega) d\omega \\ &= \int_{-\infty}^{\infty} (V_{x,inj}(\omega) - V_{y,inj}(\omega)) \cdot V_r^*(\omega) d\omega \\ &= \left(\frac{1-T(\omega_c)}{1+T(\omega_c)} \cdot \vec{v}_{rm} \cdot \vec{v}_{rm}{}^* + \frac{1-T(-\omega_c)}{1+T(-\omega_c)} \cdot \vec{v}_{rm} \cdot \vec{v}_{rm}{}^* \right) \\ &= 2 \left\| \vec{v}_{rm} \right\|^2 \cdot \mathrm{Re} \left[\frac{1-T(\omega_c)}{1+T(\omega_c)} \right] \end{aligned} \tag{5.13}$$

It is now easy to see that inner product (5.13) vanishes if and only if the loop gain at the perturbation frequency has unity magnitude. In other words, tuning objective (5.7) is achieved if and only if v_x,-v_y and v_r are orthogonal. From the foregoing considerations, the following conditions are found to be equivalent to the tuning objective (5.7):

$$\begin{aligned} \left\| T(\omega_c) \right\| = 1 &\Leftrightarrow (v_x - v_y) \perp v_r \\ &\Leftrightarrow (v_{x,inj} - v_{y,inj}) \perp v_r \end{aligned} \tag{5.14}$$

The last part of the implication is especially interesting as it involves only sinusoidal quantities, therefore reducing the tuning objective (5.7) to an orthogonality

problem between phasors. In the following section, a phasor analysis is employed to define the tuning error ε and further discuss the proposed tuning approach

5.3.2 Tuning Error

The key point to understand how the tuning error is derived in the proposed method is the result (5.14), i.e. the fact that condition (5.7) holds if and only if $v_{x,inj}$-$v_{y,inj}$ and v_r are orthogonal. This fact is graphically illustrated by the phasor diagram shown in Fig. 5.3, which reports the phasor relationships and orientations when (5.7) is satisfied. The phasors representing the signals $v_{x,inj}$ and $v_{y,inj}$ are set around the reference phasor of the perturbation signal v_r. Since the orthogonality condition shown by the phasor diagram in Fig. 5.3 represents the end objective of the tuning process, amplitude comparison of the phasors $\vec{v}_{x,inj}$ and $\vec{v}_{y,inj}$ can be performed by projecting phasors $\vec{v}_{x,inj}$ and $\vec{v}_{y,inj}$ onto the reference phasor $\vec{v}_r$; a proper definition of the tuning error is therefore the projection of $\vec{v}_{x,inj} - \vec{v}_{y,inj}$ onto $\vec{v}_r$, i.e.:

$$\varepsilon_{phasor} = (\vec{v}_{x,inj} - \vec{v}_{y,inj}) \bullet \vec{v}_r \tag{5.15}$$

where ε_{phasor} represents the tuning error derived from the phasor analysis, and the dot denotes the inner product between phasors. Tuning error (5.15) can be expressed as:

$$\varepsilon_{phasor} = \|\vec{v}_r\| \cdot (\|\vec{v}_{x,inj}\| \cdot \cos\theta_x - \|\vec{v}_{y,inj}\| \cdot \cos\theta_y) \tag{5.16}$$

It remains to show that the sign of the produced error signal (5.16) indicates whether the loop gain magnitude is greater than or less than 1. As illustrated in Fig. 5.4, if a circumscribed circle is drawn around the upper triangle of Fig. 5.3, the relationship between the phases θ_x, θ_y and the magnitudes of the phasors $\vec{v}_{x,inj}$, $\vec{v}_{y,inj}$ in (5.16) can be clarified. During the tuning process, both the magnitude of the reference phasor $\vec{v}_r$

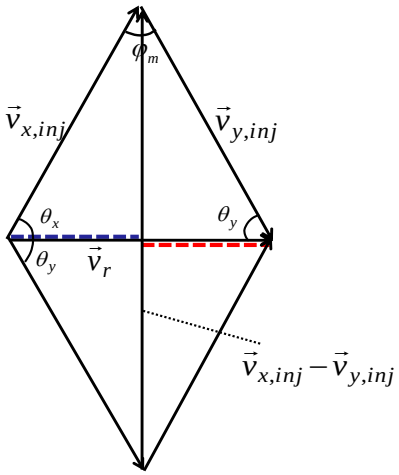
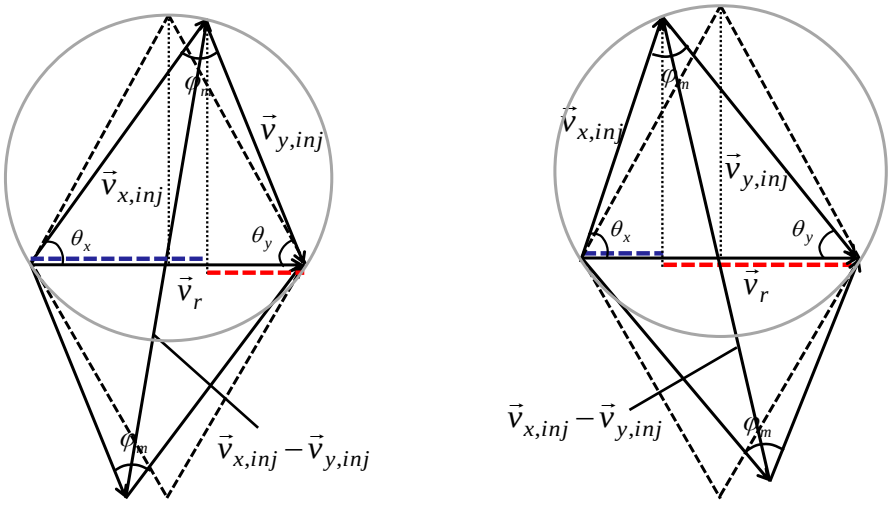


Fig. 5.3. Phasor diagram for ||T||=1



(a) $||v_{x,inj}||>||v_{y,inj}||$
$||T||<1$

(b) $||v_{x,inj}||<||v_{y,inj}||$
$||T||>1$

Fig. 5.4. Phasor diagram for $||T|| \neq 1$

and the quantity $\theta_x+\theta_y=\varphi_m$ remain constant, while phases θ_x and θ_y vary according to the magnitudes of the opposite phasors $\vec{v}_{x,inj}$ and $\vec{v}_{y,inj}$ respectively. In Fig. 5.4(a), when the loop gain magnitude is less than 1, e.g. due to a positive tolerance of the power stage parameter (L for the current loop, C for the voltage loop), the magnitude of $\vec{v}_{x,inj}$ becomes larger than that of $\vec{v}_{y,inj}$; simultaneously, θ_x decreases while θ_y increases. Thus, the first term $||\vec{v}_{x,inj}||cos\theta_x$ in (5.16) becomes larger than the second term $||\vec{v}_{y,inj}||cos\theta_y$, thereby producing a positive error. This positive tuning error is then used to increase the compensator gain until the phasor diagram aligns to the nominal operating condition, which is shown in dotted lines in Fig. 5.4(a). The opposite case, when the loop gain magnitude is greater than 1, is shown in Fig. 5.4(b) and produces a negative tuning error. Hence, since ε_{phasor} monotonically varies according to the difference of $||\vec{v}_{x,inj}||$ and $||\vec{v}_{y,inj}||$, it provides a consistent measure of the tuning error. Furthermore, this error signal can be obtained using simple arithmetic computations, as discussed in the next subsection.

5.3.3 Tuning Module Realization

Detailed signal processing in the tuning module is illustrated in Fig. 5. In the tuning module structure in Fig. 5.5, input signals are v_x, v_y, and v_r. Expressions for these time domain inputs are the same as in the phasor analysis except that remaining signal components (at frequencies other than the injection frequency) are added,

$$v_r = \left\| v_r \right\| \cdot \sin\omega_c t \tag{5.17}$$

$$v_x = V_{x,other} + \left\| v_{x,inj} \right\| \cdot \sin(\omega_c t + \theta_x) \tag{5.18}$$

$$v_y = V_{y,other} + \left\| v_{y,inj} \right\| \cdot \sin(\omega_c t + \theta_y) \tag{5.19}$$

In the current-loop tuner, large signal terms $V_{x,other}$, $V_{y,other}$ represent the duty cycle command plus some other frequency components. In the voltage-loop tuner, these signals represent the power command plus some other frequency components. In the tuning module, the three signals (5.17-5.19) go through multiplication blocks, resulting in

$$v_x \cdot v_r = \left\{ V_{x,other} + \left\| v_{x,inj} \right\| \cdot \sin(\omega_c t + \theta_x) \right\} \cdot \left\| v_r \right\| \cdot \sin \omega_c t \tag{5.20}$$

$$v_y \cdot v_r = \left\{ V_{y,other} + \left\| v_{y,inj} \right\| \cdot \sin(\omega_c t + \theta_y) \right\} \cdot \left\| v_r \right\| \cdot \sin \omega_c t \tag{5.21}$$

These two signals (5.20) and (5.21) are then subtracted to remove the other frequency components terms,

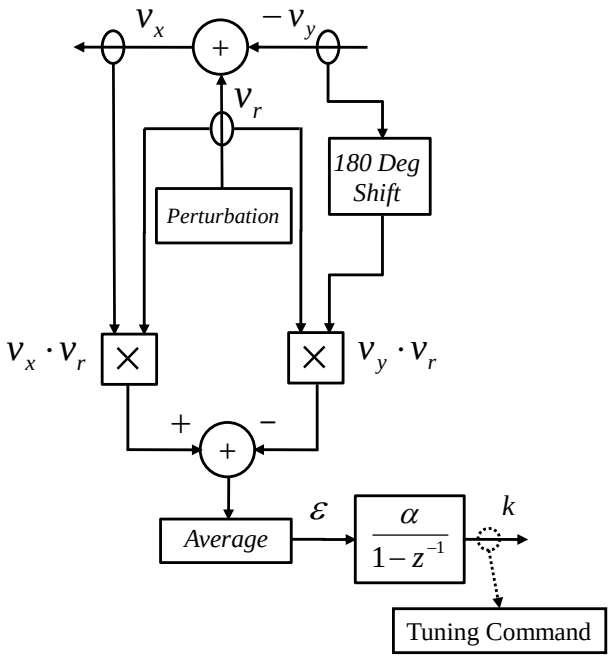


Fig. 5.5. Block diagram of the proposed auto-tuner

$$\begin{aligned} v_x \cdot v_r - v_y \cdot v_r = &\left\| v_{x,inj} \right\| \cdot \left\| v_r \right\| \cdot \sin(\omega_c t + \theta_x) \cdot \sin \omega_c t \\ &- \left\| v_{y,inj} \right\| \cdot \left\| v_r \right\| \cdot \sin(\omega_c t + \theta_y) \cdot \sin \omega_c t \end{aligned} \tag{5.22}$$

Equation (5.22) can be re-arranged,

$$\begin{aligned} v_x \cdot v_r - v_y \cdot v_r = &\frac{1}{2}(\left\| v_{x,inj} \right\| \cdot \left\| v_r \right\| \cdot \cos\theta_x - \left\| v_{y,inj} \right\| \cdot \left\| v_r \right\| \cdot \cos\theta_y) \\ &- \frac{1}{2}\left\| v_{x,inj} \right\| \cdot \left\| v_r \right\| \cdot \cos(2\omega_c t + \theta_x) + \frac{1}{2}\left\| v_{y,inj} \right\| \cdot \left\| v_r \right\| \cdot \cos(2\omega_c t + \theta_y) \end{aligned} \tag{5.23}$$

In (5.23), the last two terms contain components at twice the injection frequency. These components can be removed by averaging over an injection frequency period, to obtain

$$\varepsilon = \frac{1}{2}\left\| v_r \right\| \cdot (\left\| v_{x,inj} \right\| \cdot \cos\theta_x - \left\| v_{y,inj} \right\| \cdot \cos\theta_y) = \frac{\varepsilon_{phasor}}{2} \tag{5.24}$$

Notice that (5.24) is exactly the same as the error expression (5.16) derived from the phasor analysis except for a constant multiplicative factor of 1/2. Therefore, the tuning block indeed performs the function described in the phasor analysis. The integrator block, which accumulates the error, serves as an integral compensator in the tuning loop. The output of the integrator adjusts the compensator gains to null the error, i.e. to satisfy the tuning objective (5.7).

Moreover, the tolerance of *L* or *C* can be indirectly measured by observing the tuning command *k* since it is multiplied to the compensator gain to cancel the tolerance effect on the loop gain. In case of *L*, it can be used for accurate CCM/DCM boundary detection, as described in Chapter 6.

5.3.4 Compensator Gain Modulation

Compensator gain adjustment is another task in the proposed tuning approach. Even though the tuning module produce the tuning error command corresponding filter components tolerances, it is not obvious how the compensator gain should be adjusted. The general expression for the PI compensator is presented and modified as required to be compatible with the tuning module. The general expression for the discrete-time domain compensator is

$$G_c(z) = K_P + \frac{K_I}{(1-z^{-1})} + K_D(1-z^{-1}) \tag{5.25}$$

The PI compensator reduced to

$$G_{cPI}(z) = K_P + \frac{K_I}{(1-z^{-1})} = (K_P + K_I)\frac{(z - \frac{K_I}{K_P + K_I})}{(z-1)} \tag{5.26}$$

To adjust the gain, the tuning command, from the tuning module should only change the gain term (K_p+K_i), not the pole or zero places. If we substitute the proportional gain K_p to $k \cdot K_p$, integral gain K_i to $k \cdot K_i$, then compensator z-domain expression becomes

$$G_c(z) = k \cdot K_P + \frac{k \cdot K_I}{(1-z^{-1})} = k(K_P + K_I)\frac{(z - \frac{K_I}{K_P + K_I})}{(z-1)} \tag{5.27}$$

The constant value k is the accumulated error from the tuning module to modify the compensator gain against the variations of L or C. As shown in the equation (5.27), k multiplications to the proportional, integral gain do not change the locations of pole or zero, but the gain of the compensator. This characteristic

significantly simplifies the implementation of the compensator gain adjustment algorithm into the hardware.

5.4 Tuning Loop Modeling and Design

This section addresses dynamic modeling and design of the tuning loops. As shown in Fig. 5.6, the small-signal tuning loop gain T_{tuning} includes two blocks, the tuning loop integral (I) compensator and the small signal response from the tuning command k to the negative error signal $-\varepsilon$. The tuning loop integral (I) compensator gain α is a design parameter, which determines the speed and the stability of the tuning loop. The tuning loop gain can be written as

$$T_{tuning} = G_{k\varepsilon} \cdot \frac{\alpha}{1 - z^{-1}} \tag{5.28}$$

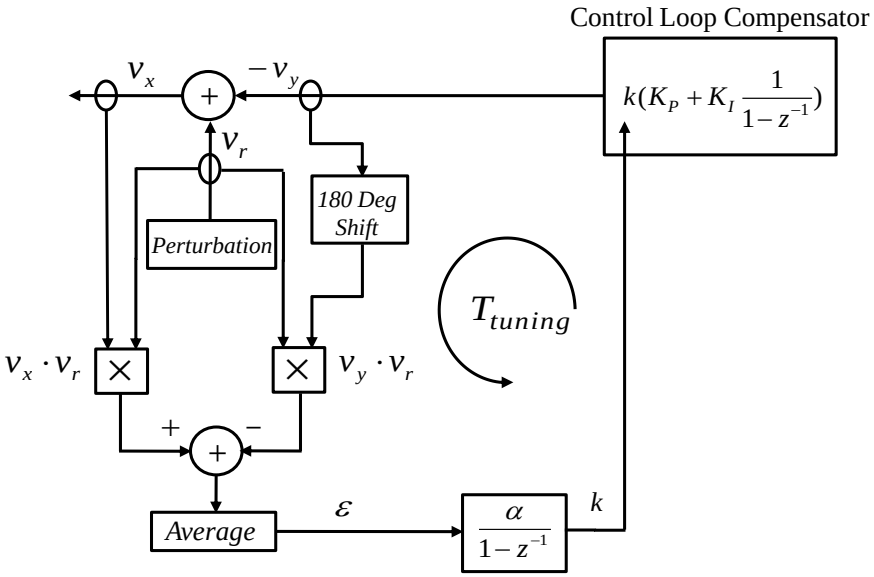


Fig. 5.6. Block diagram of the tuning loop

where $G_{k\varepsilon}$ is the small signal response of -ε to the k variation,

$$G_{k\varepsilon} = \hat{k} \rightarrow -\hat{\varepsilon} \tag{5.29}$$

The response $G_{k\varepsilon}$ can be derived based on the assumption that the current or voltage control loop is much faster than the corresponding tuning loop. As shown in Fig. 7, this assumption implies that the sampling rate $T_{sampling}$ in the tuning loop is much longer than transients in ε associated with changes in k [34]. As a result, upon an update in k, dynamics in the tuning loop can be ignored, and the sampled error $\varepsilon[n]$ can be obtained as a steady-state response. Therefore, the transfer function $G_{k\varepsilon}$ can be represented by gain and delay terms as

$$G_{k\varepsilon}(z) = \frac{A_{k\varepsilon}}{z_t} \tag{5.30}$$

where z_t corresponds to sampling at $T_{sampling}$

$$z_t = e^{sT_{sampling}}, \tag{5.31}$$

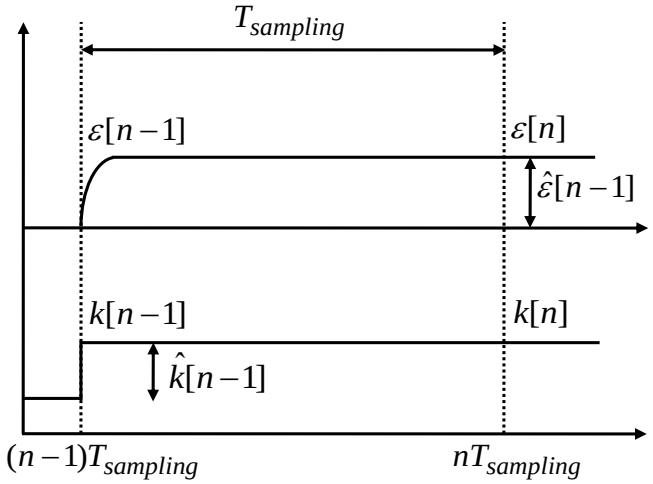


Fig. 5.7. Waveforms illustrating k, ε, and sampling instance

and $A_{k\varepsilon}$ is a simple gain.

For the purpose of the derivation of the gain term $A_{k\varepsilon}$, the relationship between k and ε is derived from the geometric representation of the signals in Fig. 5.3. By applying the cosine law, relations between the signals can be written as

$$\begin{aligned} \left\|\vec{v}_r\right\|^2 &= \left\|\vec{v}_{x,inj}\right\|^2 + \left\|\vec{v}_{y,inj}\right\|^2 - 2\left\|\vec{v}_{x,inj}\right\|\cdot\left\|\vec{v}_{y,inj}\right\|\cdot\cos\varphi_m \\ \left\|\vec{v}_{y,inj}\right\|^2 &= \left\|\vec{v}_{x,inj}\right\|^2 + \left\|\vec{v}_r\right\|^2 - 2\left\|\vec{v}_r\right\|\cdot\left\|\vec{v}_{x,inj}\right\|\cdot\cos\theta_x \\ \left\|\vec{v}_{x,inj}\right\|^2 &= \left\|\vec{v}_{y,inj}\right\|^2 + \left\|\vec{v}_r\right\|^2 - 2\left\|\vec{v}_r\right\|\cdot\left\|\vec{v}_{y,inj}\right\|\cdot\cos\theta_y \end{aligned} \tag{5.32}$$

From (5.24), (5.32), the error signal ε can be expressed as a function of tuning command k

$$\begin{aligned} \varepsilon &= \frac{(1-\dfrac{\left\|\vec{v}_{y,inj}\right\|^2}{\left\|\vec{v}_{x,inj}\right\|^2})\cdot\left\|v_r\right\|^2}{2(1+\dfrac{\left\|\vec{v}_{y,inj}\right\|^2}{\left\|\vec{v}_{x,inj}\right\|^2}-2\dfrac{\left\|\vec{v}_{y,inj}\right\|}{\left\|\vec{v}_{x,inj}\right\|}\cdot\cos\varphi_m)} = \frac{(1-\left\|T\right\|^2)\cdot\left\|\vec{v}_r\right\|^2}{2(1+\left\|T\right\|^2-2\left\|T\right\|\cdot\cos\varphi_m)} \\ &= \frac{\left[1-(\left\|T_{initial}\right\|\cdot k)^2\right]\cdot\left\|\vec{v}_r\right\|^2}{2\left[1+(\left\|T_{initial}\right\|\cdot k)^2-2(\left\|T_{initial}\right\|\cdot k)\cdot\cos\varphi_m\right]} \end{aligned} \tag{5.33}$$

where the control loop gain T is defined in (5.6), and $T_{initial}$ represents the initial current or voltage loop gain before tuning. The default value for k is 1. Therefore, the ideal target value for $||T_{initial}||K$ after tuning is unity, where K is the steady state value of the gain. The gain term $A_{k\varepsilon}$ can be calculated by taking a derivative of (5.33) with respect to k,

$$\begin{aligned} A_{k\varepsilon} &= -\left.\frac{\partial\varepsilon(k)}{\partial k}\right|_{k=K} \\ &= \frac{(-\left\|T_{initial}\right\|^3\cdot\cos\varphi_m\cdot K^2+2\left\|T_{initial}\right\|^2\cdot K-\left\|T_{initial}\right\|\cdot\cos\varphi_m)\cdot\left\|\vec{v}_r\right\|^2}{\left[1+(\left\|T_{initial}\right\|\cdot K)^2-2\left\|T_{initial}\right\|\cdot K\cdot\cos\varphi_m\right]^2} \end{aligned} \tag{5.34}$$

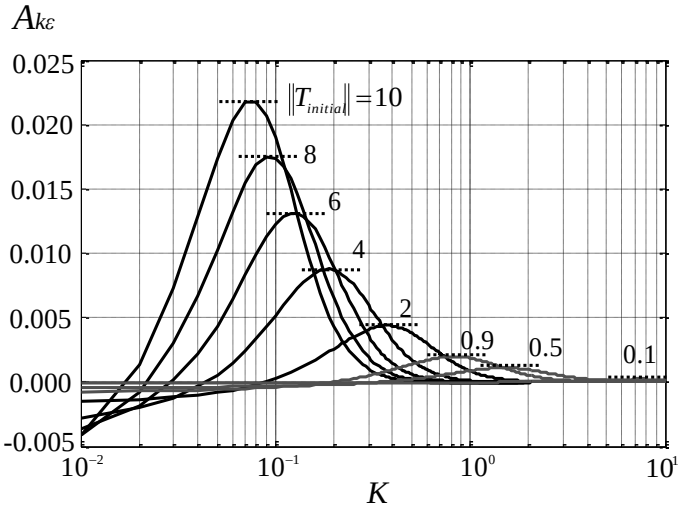


Fig. 5.8. The gain term $A_{k\varepsilon}$ plot for different $||T_{initial}||$ values (0.1~10) (φ_m=70°, $\|\vec{v}_r\|=0.05$)

Note that $||T_{initial}||$ represents an uncertainty in the initial value of the control loop gain.

The tuning loop design consists of selecting the integral gain α to ensure stability and well-behaved dynamic response of the tuning loop for a given range $||T_{initial}||$. It is therefore of interest to find how $A_{k\varepsilon}$ depends on K and $||T_{initial}||$. Fig. 5.8 shows the gain term $A_{k\varepsilon}$ behavior as a function of K when $||T_{initial}||$ range is set as 0.1~10. For a specific $||T_{initial}||$ value, there is a value of K where the gain $A_{k\varepsilon}$ attains a peak value, namely $A_{k\varepsilon\_peak}$. Fig. 5.9 shows how $A_{k\varepsilon\_peak}$ increases with $||T_{initial}||$. Therefore, for the design of the tuning loop the worst-case gain $A_{k\varepsilon\_max}$ can be found as $A_{k\varepsilon\_peak}$ corresponding the upper limit of $||T_{initial}||$. For example, assuming $||T_{initial}||$ = 10, which corresponds to the initial loop gain uncertainty of up to 10 times

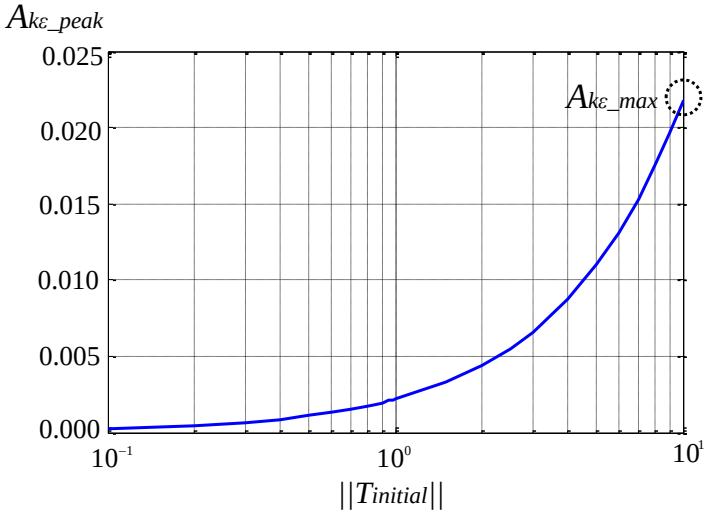


Fig. 5.9. Peak $A_{k\varepsilon}$ value ($A_{k\varepsilon\_peak}$) for each $||T_{initial}||$ value (φ_m=70°, $\|\bar{v}_r\| = 0.05$)

the nominal loop gain, Fig. 5.9 shows that $A_{k\varepsilon\_max}$ = 0.0218. The worst-case tuning loop gain then becomes

$$T_{tuning} = A_{k\varepsilon\_\max} \cdot \frac{\alpha}{z_t - 1} \tag{5.35}$$

A larger α corresponds to a faster tuning process. The worst-case loop gain (5.35) can be used to select a maximum α to guarantee stable and well behaved operation of the tuning loop. Design examples are given in Section 5.5.

5.5 Experimental Results

The boost PFC rectifier prototype was built with the following parameters: $V_{g,rms}$ = 85 V_{rms} ~ 260 V_{rms}, f_{line} = 50 Hz, V_o = 380 V, f_s =100 kHz, L = 0.5 mH, C = 220 μF, P_{av} = 75 W ~ 500 W. Digital controller was Verilog-HDL coded and implemented using a Xilinx Virtex-IV FPGA development platform.

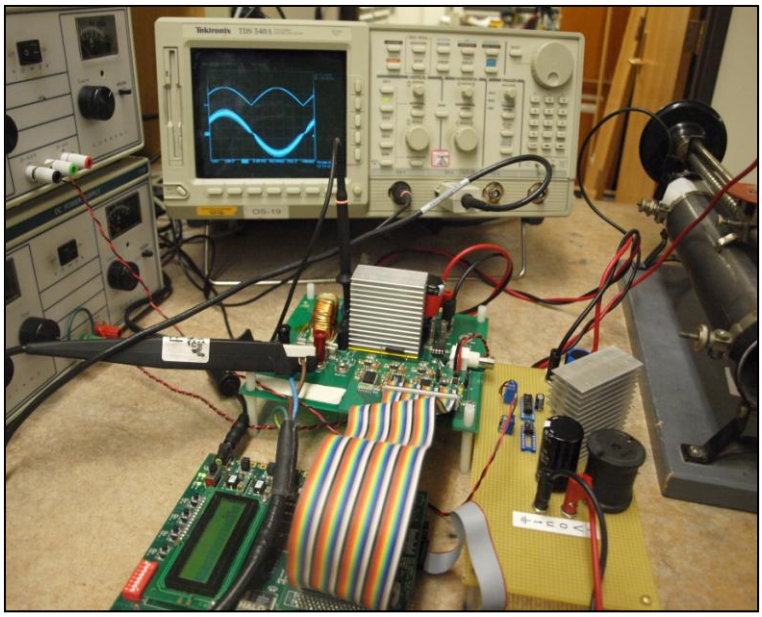


Fig. 5.10. Experimental set-up

The development board utilizes the Xilinx XC4VLX25-10FS363C FPGA operating based on the 100 MHz clock source. It supports up to 24,192 logic cells, and offers easy implementation of the complicated computations such as variable division and square root computation by adopting CORDIC (Coordinate Rotation Digital Computer) algorithm as well as arithmetic computation function.

Assuming nominal L and C values, proportional-integral (PI) compensators for both current loop and voltage loop are designed directly in discrete time domain such that the current loop has 10 kHz crossover frequency and 55˚ phase margin, and voltage loop has 5 Hz crossover frequency and 68˚ phase margin. When the system goes into DCM, the CCM compensator for the current loop is disabled, and the simple integral (I) DCM compensator is activated so that the current loop has 5 kHz bandwidth with 90° phase margin. These particular stability margins are selected for proper operation of power factor correction (PFC) rectifier in CCM and DCM. The

line frequency is 50 Hz, and the inductor current, which is the rectified input current, is periodic over twice the line period. Moreover, high frequency components at the zero crossings of the inductor current, lead to a high bandwidth of the current control loop up to a few kilohertz. The outer voltage loop, on the other hand, balances the power level of input and output ports, and regulates the output voltage as far as it does not affect the shape of the inductor current. Hence, the outer voltage loop should have very low bandwidth generally around a few hertz. Output is loaded with a 2^{nd} stage high-bandwidth dc-dc buck voltage regulator, which can be modeled as a 300 W power sink.

Since the tuner is designed to operate only in CCM, the system should be working in CCM at least during the tuning process. For each loop, tuner injects the sinusoidal perturbation signal amplitude set to 5% of the maximum control command magnitude, at 10 kHz for the current loop, and 5% of the nominal control command magnitude, at 5 Hz for the voltage loop.

The perturbations are generated as sampled versions of continuous sinusoidal waves. In the current control loop, since the controller is designed to compute the new duty cycle every 10 μs, the perturbation sampling rate of 100 kHz is sufficiently high. Thus, 10 kHz current loop perturbation signal consists of 10 samples of sinusoidal wave per one perturbation cycle.

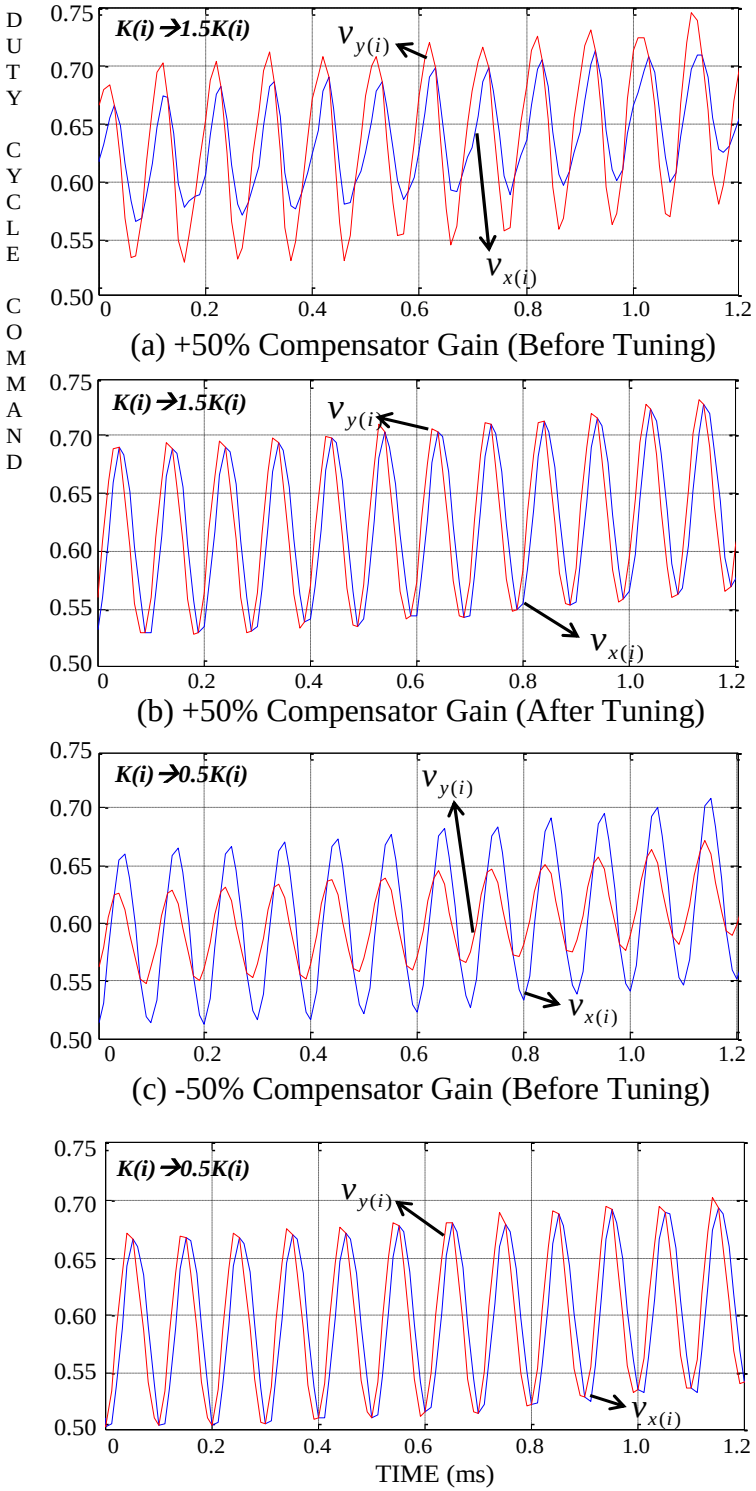
The voltage loop perturbation is also based on 10 samples of the sinusoidal wave per cycle. For the current tuning loop, the tuning module sampling rate is set to 100 Hz, which is twice the line cycle. The average value of 10 error signals ε taken near the sampling instance represents the final error signal ε. For the voltage tuning

loop, the tuning module sampling rate is set to 2.5 Hz. The representing error signal ε, in this case, is the average value of 20 error signals sampled around the sampling instance.

The proposed tuner was tested for different initial compensator gains and for a ±50% deviation in the power stage parameters. Fig. 5.11 - 5.14 show signals v_x and v_y before and after tuning for an extreme case of ±50% tolerances in L and C and ±50% of initial operating condition. It can be observed how the tuner is always capable of equalizing amplitudes of the $v_{x,inj}$ and $v_{y,inj}$ signal perturbations, reaching the tuning objective (5.7).

Experimental results for the voltage loop tuning are shown in Fig. 5.15. When the voltage loop compensator gain is initially set to 1.5 times the nominal compensator gain, the output voltage transient response to the output power step from 300 W to 200 W is shown in Fig. 5.15(a). An improved transient response corresponding to improved phase margin after tuning can be observed in Fig. 5.15(b). Fig 5.16 shows the voltage loop tuning results for 220 V_{rms} input voltage under the same condition as in Fig 5.15, implying that the tuning technique is compatible with the universal input voltage.

Fig. 5.17 illustrates an experimental example of the current loop tuning process. Initially, current loop compensator gain is set to 1/10 of the nominal value, resulting in a fairly distorted current waveshape as shown in Fig. 5.17(a). The feedback system then goes through perturbation and tuning, which are depicted in Fig. 5.17(b) and 5.17(c) respectively. Fig. 5.17(d) illustrates the post-tuning behavior, in which the current loop bandwidth has been adjusted to the nominal value. The comparison of



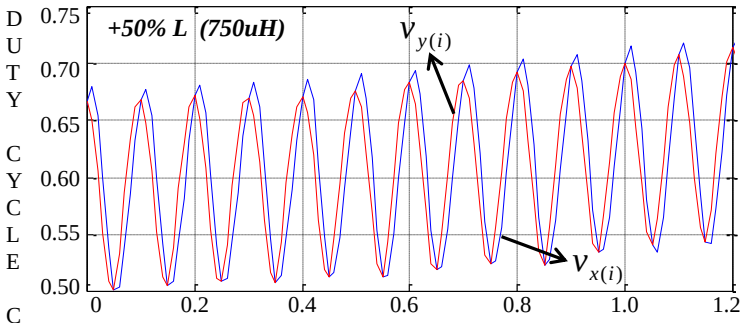
(a) +50% Compensator Gain (Before Tuning)

(b) +50% Compensator Gain (After Tuning)

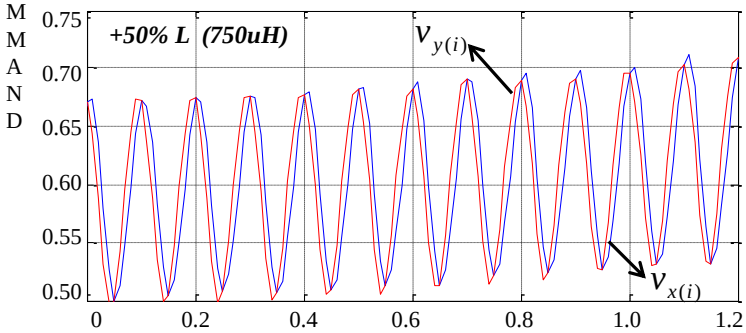
(c) -50% Compensator Gain (Before Tuning)

(d) -50% Compensator Gain (After Tuning)

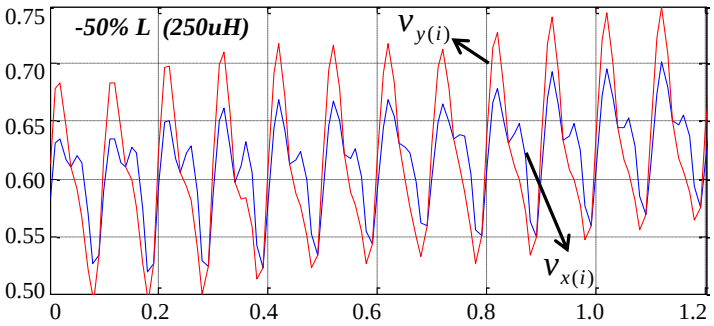
Fig 5.11. Magnitude ratios of $v_{x(i)}$ and $v_{y(i)}$ of current loop in the existence of ±50% of initial compensator gain. ($v_{x(i)}$,$v_{y(i)}$-0.05/Div, time-0.2ms/Div)



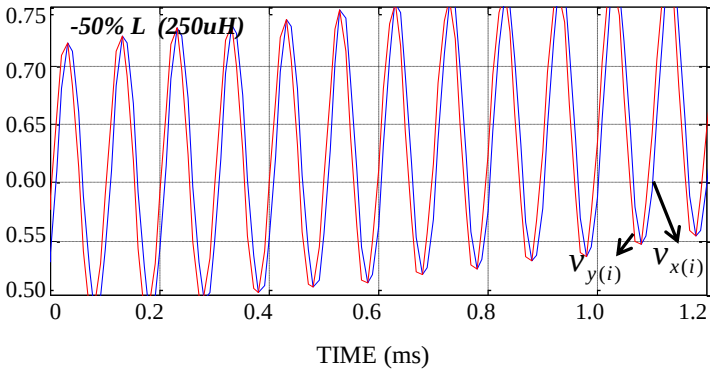
(a) +50% *L* tolerance (Before Tuning)



(b) +50% *L* tolerance (After Tuning)

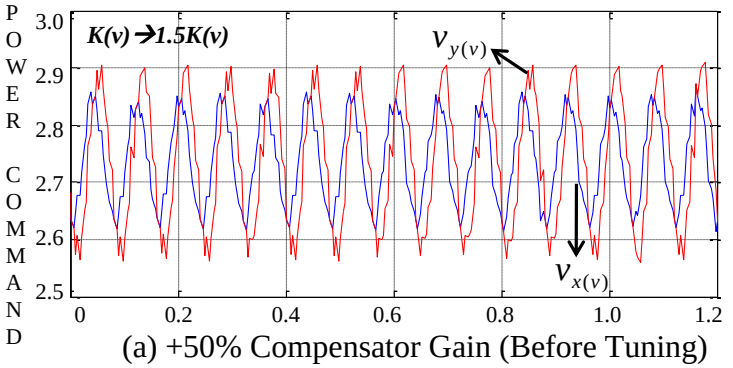


(c) -50% *L* tolerance (Before Tuning)

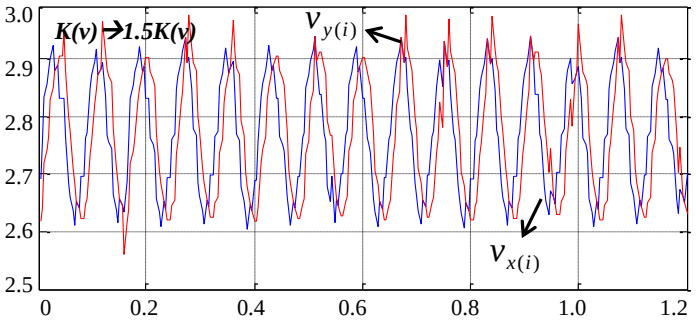


(d) -50% *L* tolerance (After Tuning)

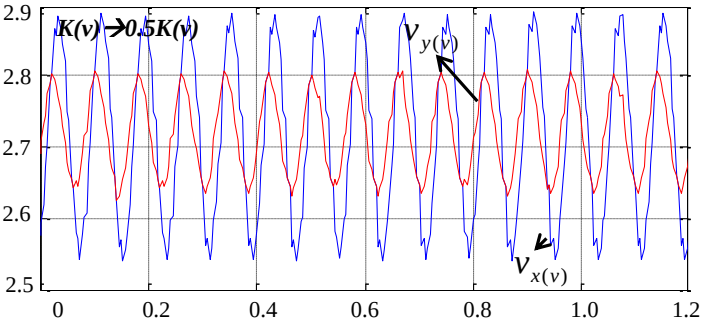
Fig 5.12. Magnitude ratios of $v_{x(i)}$ and $v_{y(i)}$ of current loop in the existence of ±50% *L* tolerances. ($v_{x(i)}$,$v_{y(i)}$-0.05/Div, time-0.2ms/Div)



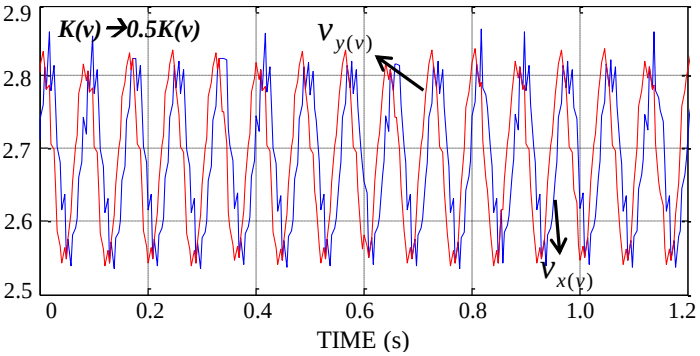
(a) +50% Compensator Gain (Before Tuning)



(b) +50% Compensator Gain (After Tuning)

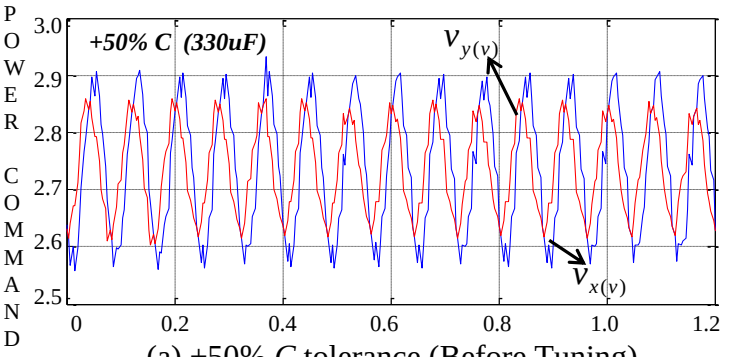


(c) -50% Compensator Gain (Before Tuning)

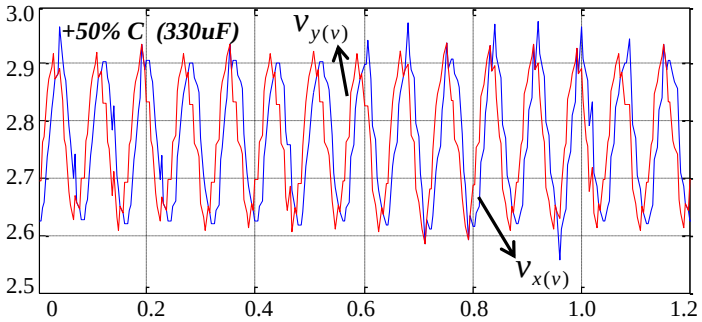


(d) -50% Compensator Gain (After Tuning)

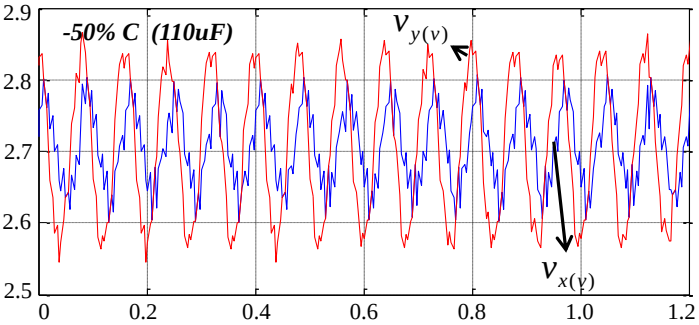
Fig 5.13. Magnitude ratios of $v_{x(v)}$ and $v_{y(v)}$ of voltage loop in the existence of ±50% of initial compensator gain. ($v_{x(v)}$,$v_{y(v)}$-0.1/Div, time-0.2ms/Div)



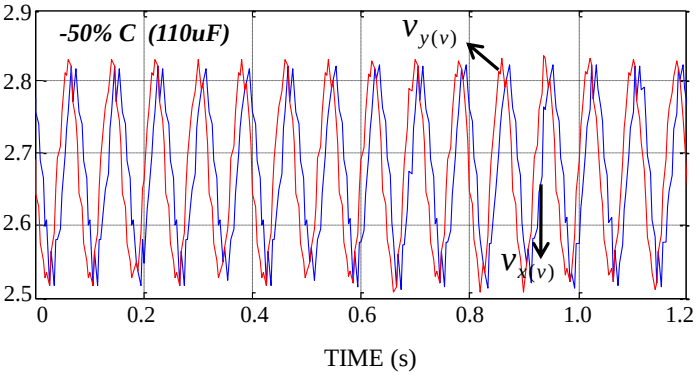
(a) +50% *C* tolerance (Before Tuning)



(b) +50% *C* tolerance (After Tuning)

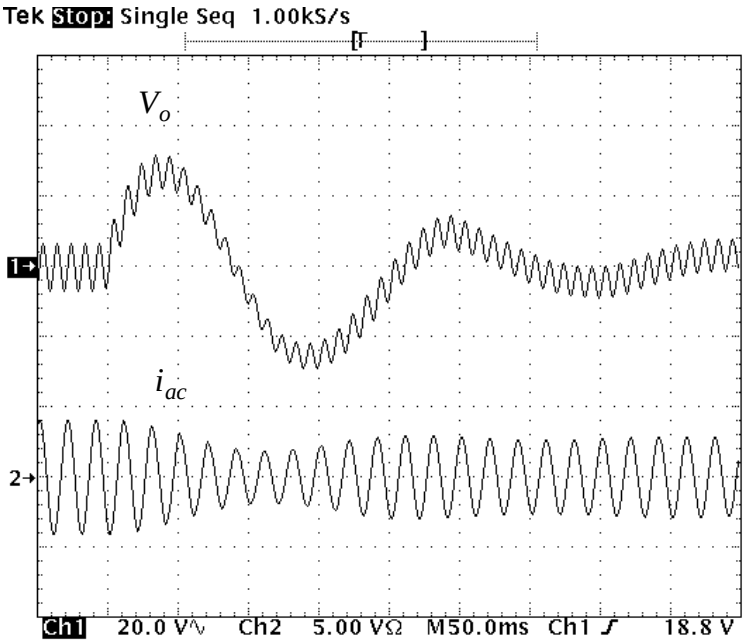


(c) -50% *C* tolerance (Before Tuning)

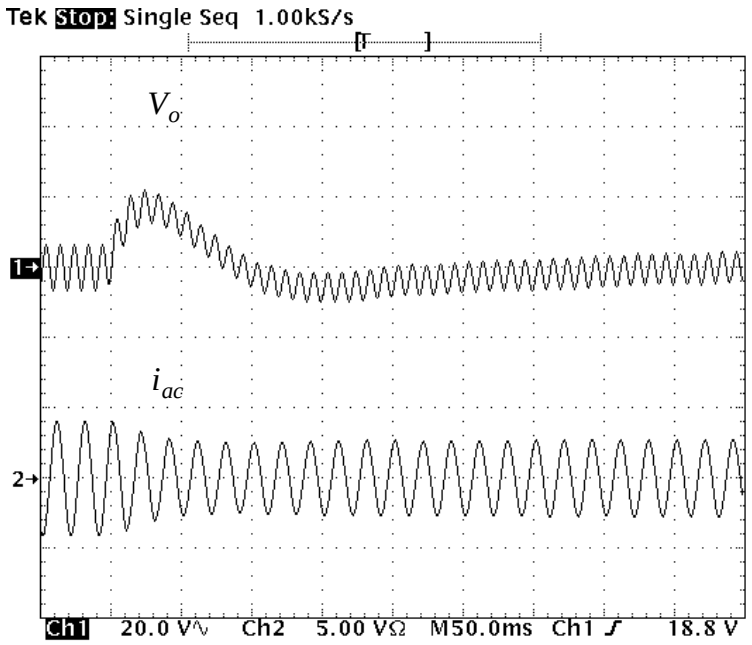


(d) -50% *C* tolerance (After Tuning)

Fig 5.14. Magnitude ratios of $v_{x(v)}$ and $v_{y(v)}$ of voltage loop in the existence of ±50% of *C* tolerances. ($v_{x(v)}$,$v_{y(v)}$-0.1/Div, time-0.2ms/Div)



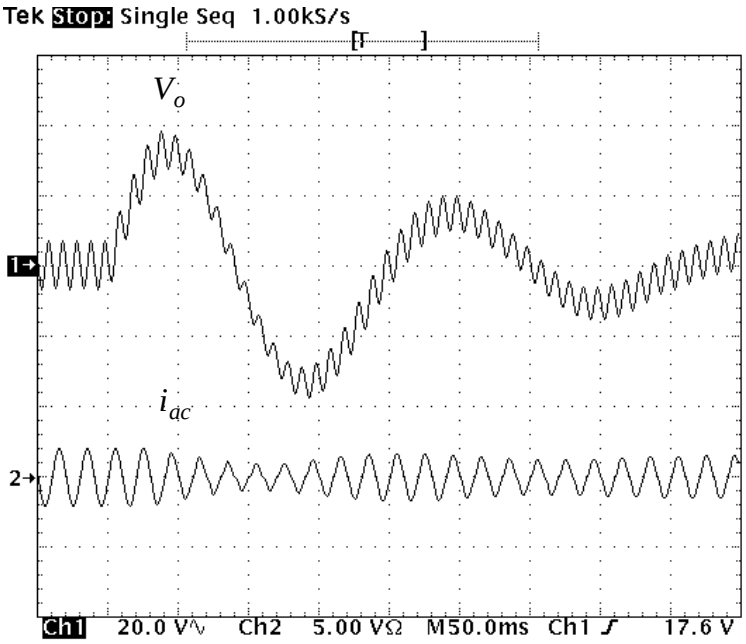
(a)



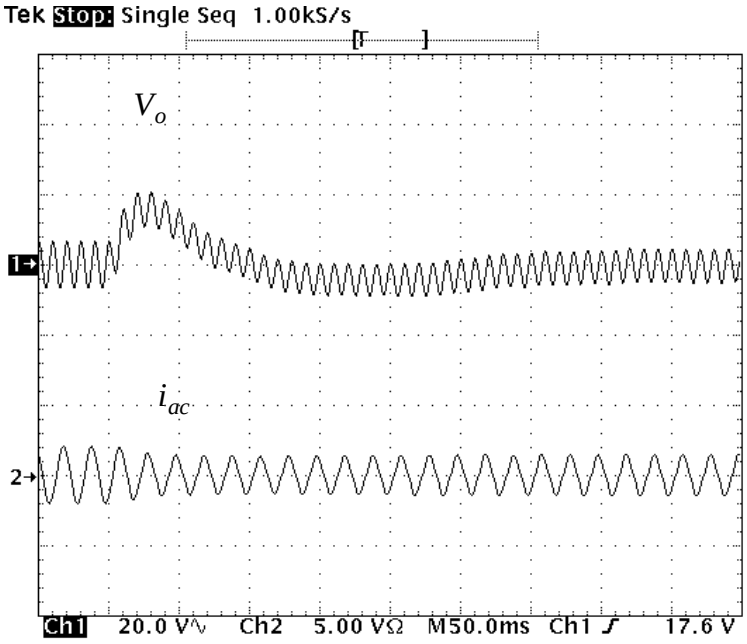
(b)

Fig. 5.15. Transient response for the output power change from 300W to 200W for (a) Before voltage loop tuning, (b) After voltage loop tuning

V_g=110V_{rms}, f_{line}=50Hz ch 1: Output voltage (V_o)-20V/Div, time-50ms/Div, ch2: AC input current (i_{ac})-5A/Div, time-50ms/Div



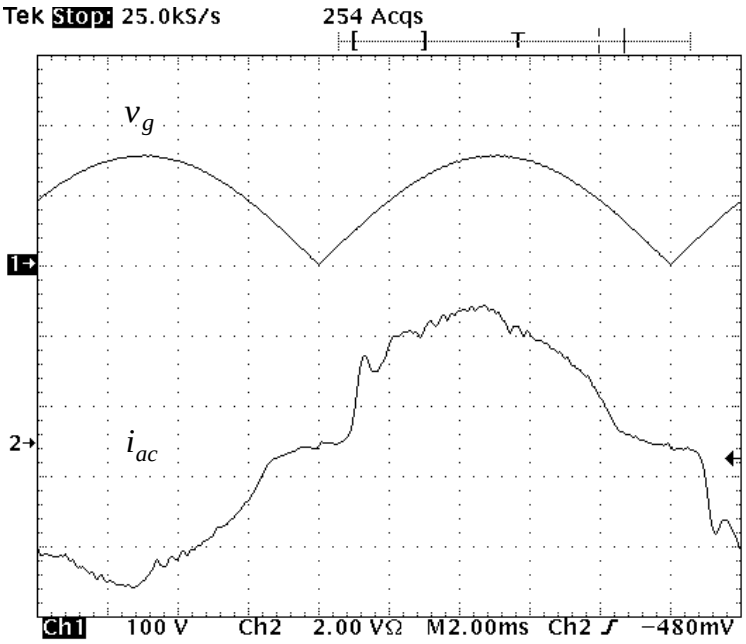
(a)



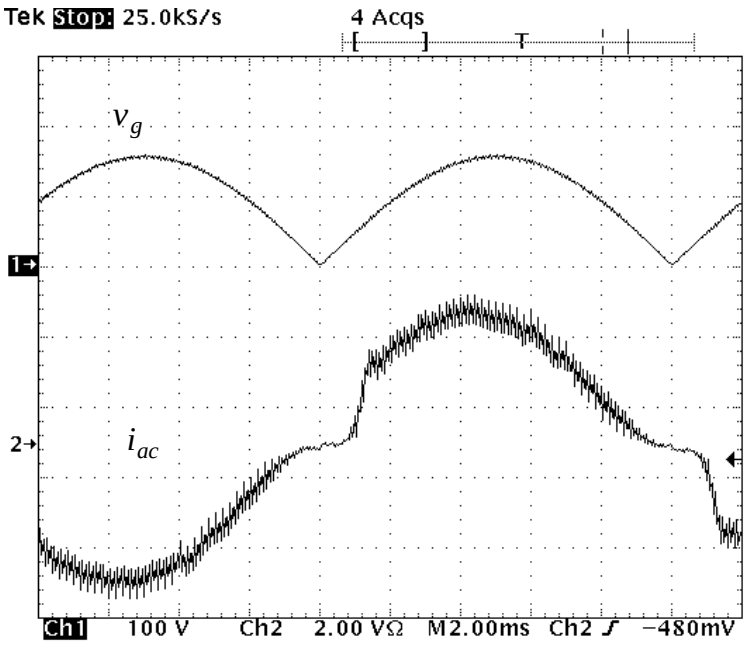
(b)

Fig. 5.16. Transient response for the output power change from 300W to 200W for (a) Before voltage loop tuning, (b) After voltage loop tuning

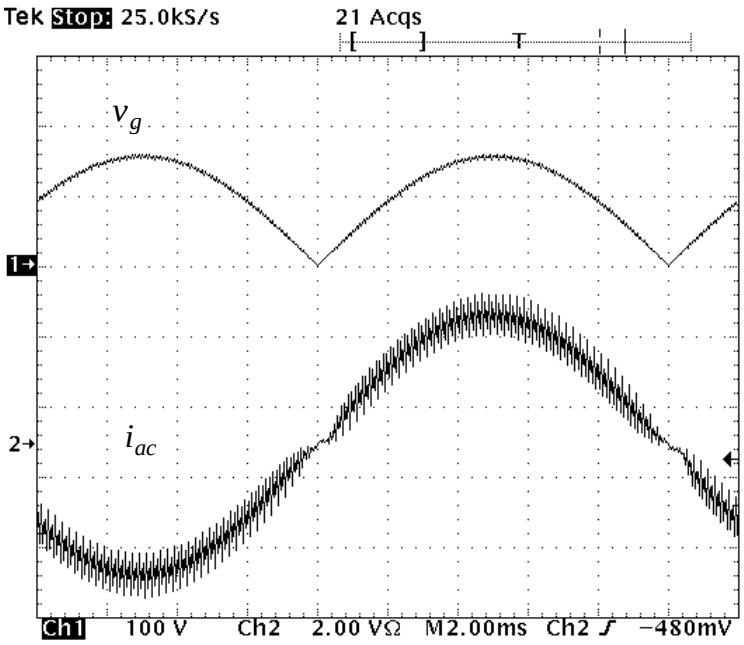
V_g=220V_{rms}, f_{line}=50Hz ch 1: Output voltage (V_o)-20V/Div, time-50ms/Div, ch2: AC input current (i_{ac})-5A/Div, time-50ms/Div



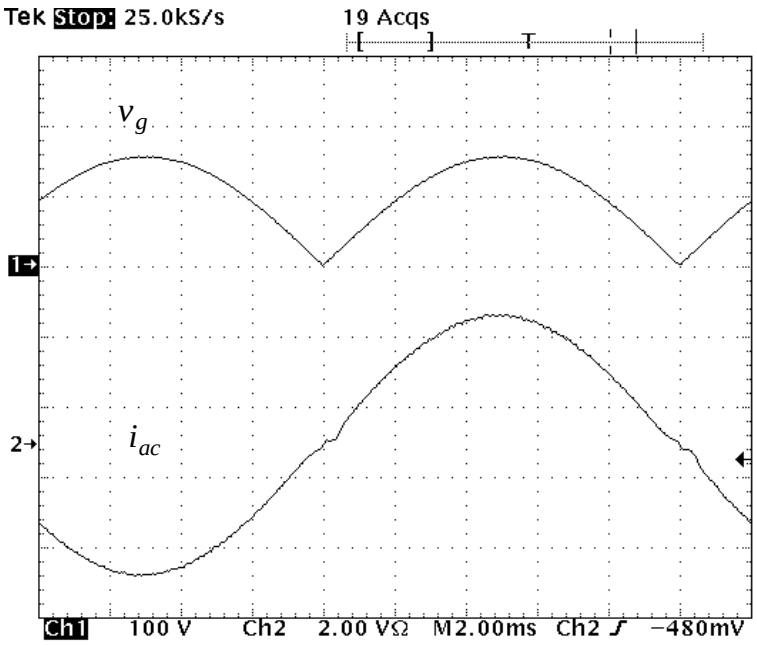
(a) Before tuning (with 1/10 of nominal compensator gain 0.1K(i))



(b) Injection of 10kHz perturbation

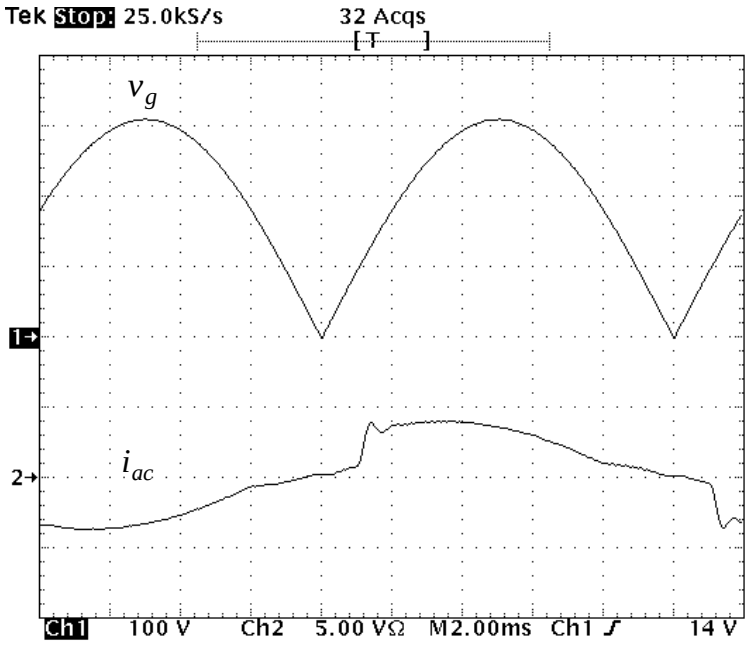


(c) Tuning is activating

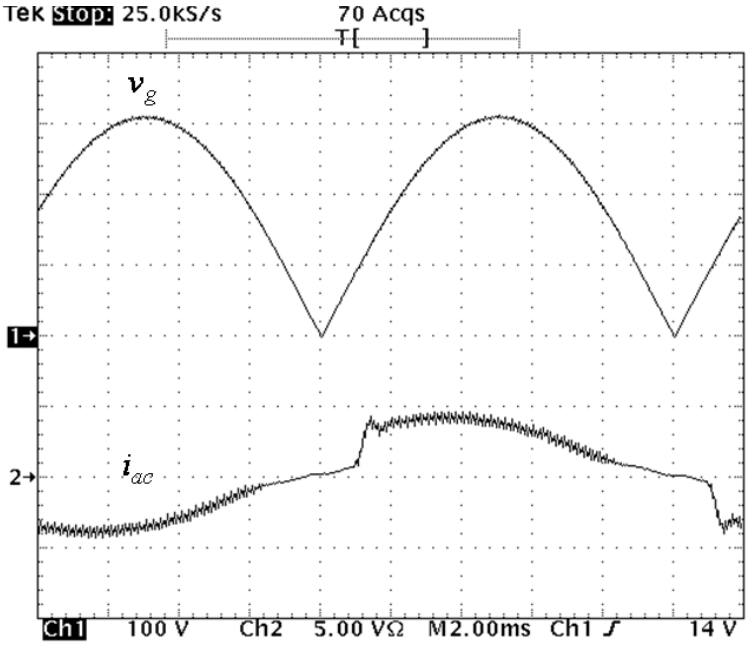


(d) After tuning

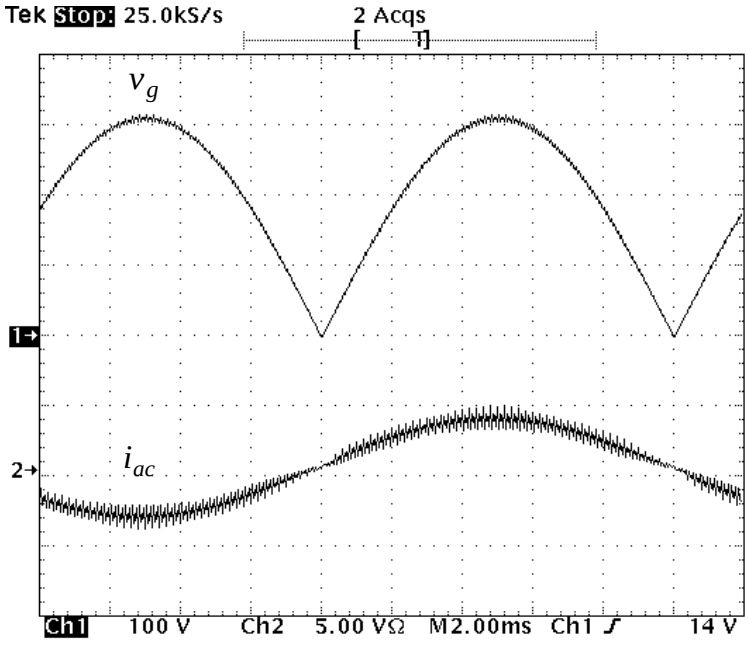
Fig. 5.17. Current loop tuning procedure
P=300W, V_g=110V_{rms}, f_{line}=50Hz Before tuning (a), On-line identification by perturbation (b), Tuning operation (c), After tuning (d).
ch1: Rectified input voltage(v_g)-100V/Div and
ch2: AC input current (i_{ac})-2A/Div, time- 2ms/Div



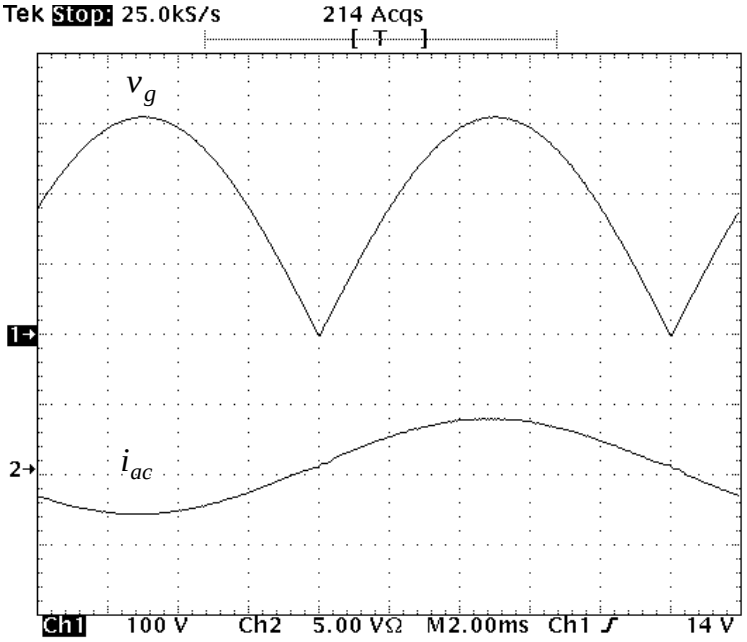
(a) Before tuning (with 1/10 of nominal compensator gain 0.1K(i))



(b) Injection of 10kHz perturbation



(c) Tuning is activating



(d) After tuning

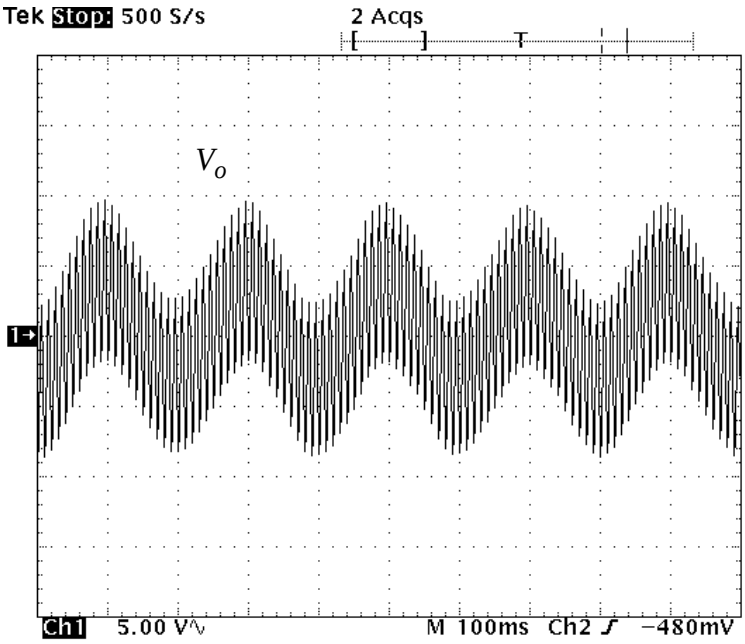
Fig. 5.18. Current loop tuning procedure
P=500W, V_g=220V_{rms}, f_{line}=50Hz Before tuning (a), On-line identification by perturbation (b), Tuning operation (c), After tuning (d).
ch1: Rectified input voltage(v_g)-100V/Div and
ch2: AC input current (i_{ac})-2A/Div, time- 2ms/Div

Fig. 5.17(a) and Fig. 5.17(d) clearly shows the capability of the tuning approach, which recovers the system operating conditions as desired. The current loop tuning result for 220 V_{rms} input voltage is also shown in Fig. 5.18.

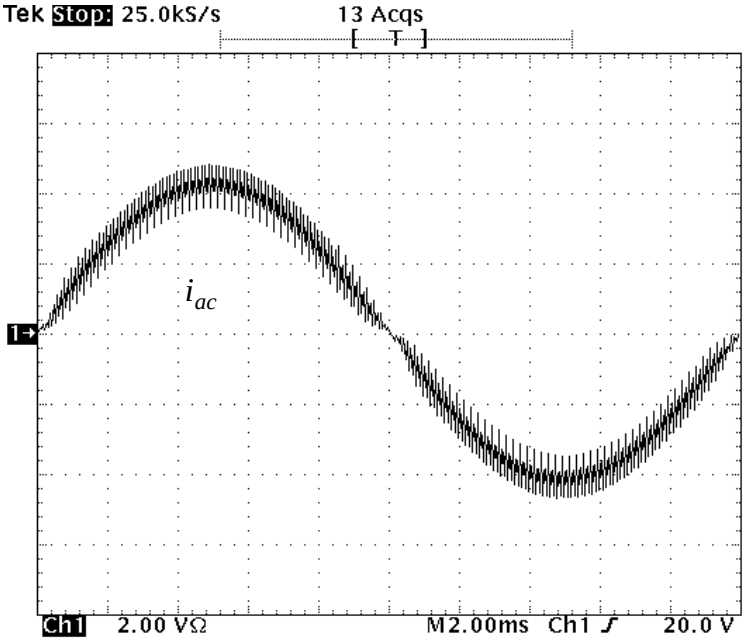
The effects of the perturbations on the output voltage and input current during voltage loop and current loop tuning are also illustrated in Fig. 5.19. The tuner activity results in small perturbations on the output voltage and the input current. Since the tuners are activated on command only when the tuning and the accurate component values are required, the normal system operation is not affected by the perturbations.

The approach is capable of handling a wide range of operating conditions, ranging from 1/20 to 3 times the nominal compensator gain. Table 5.1 summarizes the performance of the current loop tuning module at different operating conditions when the initial compensator gain is set to various relative gains with respect to the nominal gain. Table 5.2 and 5.3 compare the system performance before and after tuning for different input voltage levels.

The tuning loop is designed to achieve specific stability margins according to (5.35). Initially, $||T_{initial}||$ range is set by assuming the maximum filter component tolerance in each case for the voltage loop and the current loop is a ±50%, which corresponds to 0.5~1.5 $||T_{initial}||$ range. The tuning loop integral compensator gain α for the current loop is then set such that the current tuning loop has 1.5 Hz bandwidth and 85° phase margin with specific $A_{k\varepsilon\_max}$ value when $||T_{initial}||$ range is set to 0.5~1.5. For the voltage loop, α value is set to achieve 0.3 Hz bandwidth and 80° phase margin with $A_{k\varepsilon\_max}$ value when $||T_{initial}||$ range is set to 0.5~1.5. The tuning command k



(a)



(b)

Fig. 5.19. Perturbation signal : (a) (5Hz) on the output voltage during voltage loop tuning process. -5V/Div, time-100ms/Div , (b) (10kHz) on the input current during current loop tuning process -2A/Div, time-2ms/Div

Table 5.1: Current loop tuning module performance for various initial operating conditions

	Before Tuning		After Tuning	
Relative Gain	Power Factor	i_{ac} THD	Power Factor	i_{ac} THD
1/3	0.999	3.6%	1.000	1.9%
1/5	0.994	4.2%	1.000	1.9%
1/10	0.994	6.8%	1.000	1.9%
1/20	0.979	13.7%	1.000	1.9%
3	0.999	2.0%	1.000	1.9%

Table 5.2: Current loop post-tuning results summary

	Current Loop Tuning			
	Before Tuning		After Tuning	
Input Voltage	Power Factor	i_{ac} THD	Power Factor	i_{ac} THD
$110V_{rms}$	0.994	6.8%	1.000	1.9%
$220V_{rms}$	0.943	23.2%	0.999	1.9%

Table 5.3: Voltage loop post-tuning results summary

	Voltage Loop Tuning			
	Before Tuning		After Tuning	
Input Voltage	Maximum ΔV_o	Settling Time	Maximum ΔV_o	Settling Time
$110V_{rms}$	~30V	~400ms	~20V	~200ms
$220V_{rms}$	~30V	~400ms	~20V	~200ms

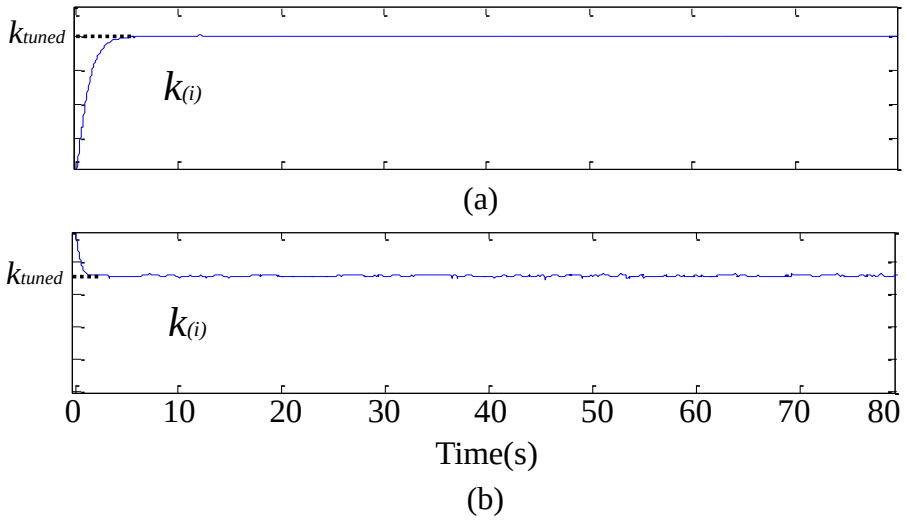


Fig. 5.20. Dynamic performance of the current tuning loop (a) tuning command $k_{(i)}$ when initial compensator gain is 1/2 of the nominal gain, (b) tuning command $k_{(i)}$ when initial compensator gain is 1.5 times the nominal gain, k_{tuned} : tuning target value for $k_{(i)}$

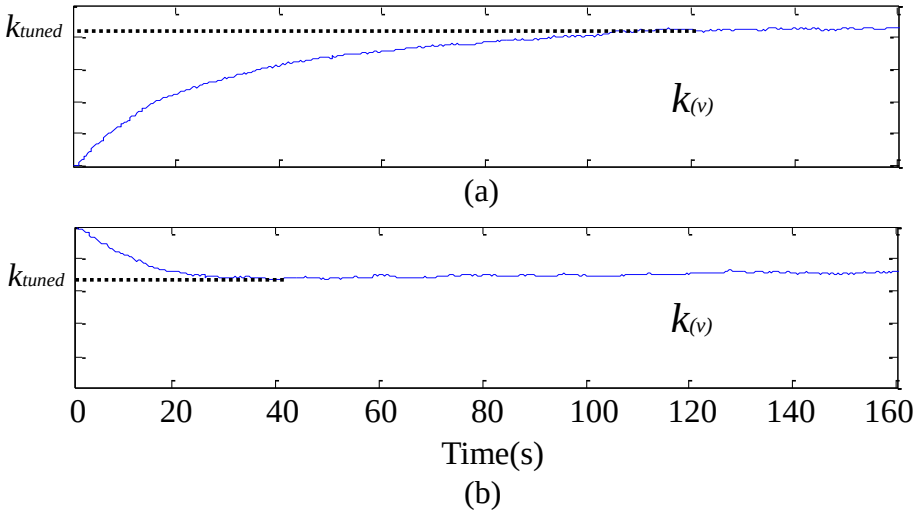


Fig. 5.21. Dynamic performance of the voltage tuning loop (a) tuning command $k_{(v)}$ when initial compensator gain is 1/2 of the nominal gain, (b) tuning command $k_{(v)}$ when initial compensator gain is 1.5 times the nominal gain, k_{tuned} : tuning target value for $k_{(v)}$

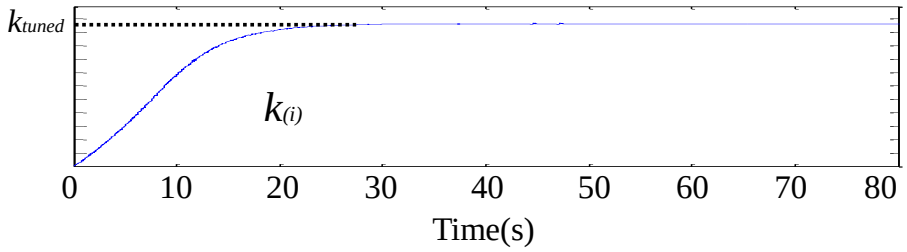


Fig. 5.22. Dynamic performance of the current tuning loop: tuning command $k_{(i)}$ with the same α value from Fig. 17 when initial compensator gain is 1/10 of the nominal gain, k_{tuned} : tuning target value for $k_{(i)}$

Table 5.4: Hardware requirements for the tuning system

	Logic Gates
Digital Average Current Mode Controller	4,499
Current Loop Tuning Module	4,615
Voltage Loop Tuning Module	3,612

behaviors, which verify stable current and voltage loop tuning operations are shown in Fig. 5.20 and 5.21. In both cases, the tuning command k values converge to the desired steady state values in a stable manner. In Fig. 5.22, it is shown that any $||T_{initial}||$ value less than the assumed upper limit of $||T_{initial}||$ range results in stable operation with the same α value obtained from the tuning loop design stage. The resolution of k determines how precisely the tuner can measure the filter component values and achieves the target stability margins. In the experiment, the resolution of k has been chosen such that the tuning command can be specified down to two decimal places. The hardware requirements for the tuning modules and the conventional controller are specified in Table 5.4.

5.6 Conclusions and Discussion

This chapter presents a robust auto-tuning approach for digitally controlled AC-DC boost power factor correction rectifiers. By simply adjusting the compensator gains, both desired crossover frequencies and phase margins are achieved for both voltage and current loops without prior knowledge of L and C.

This plug-and-play type auto-tuner guarantees the stable system operation in the presence of typical range of the passive component tolerances, spanning ±50% of the nominal value. The simple tuning algorithm features on-line estimation of the filter component values in addition to straightforward hardware implementation. The estimated inductance also can be useful information for digital current programmed control technique as further potential.

Experimental results on a 300 W digitally controlled single-phase boost power factor correction rectifier verify the proposed approach and its robustness over a wide range of operating conditions and power stage parameter tolerances.

CHAPTER 6

Accurate Mode Boundary Detection in Digitally Controlled AC-DC Boost Power Factor Correction (PFC) Rectifiers

Objectives in power factor correction (PFC) rectifiers include unity power factor and low current harmonic content in the input current. To achieve these objectives, input current should be in phase with and follow the shape of the ac input voltage. In the standard average current mode control approach, two control loops are designed to achieve the objectives: a current control loop shapes the input current in proportion to the input voltage, while a voltage control loop regulates the output voltage. Dynamics in the current control loop differ significantly depending on the operating mode: continuous conduction mode (CCM), or discontinuous conduction mode (DCM). It is difficult to maintain consistent current control loop performance in both DCM and CCM using a standard controller with fixed parameters. It is therefore advantageous to adjust the controller parameters depending on the operating mode. Such adjustment is particularly easy in programmable digital controllers [21].

At heavy loads or at light loads, the PFC rectifier operates always in CCM or always in DCM, respectively. In these cases, it is relatively easy to switch controller parameters to achieve high performance current shaping in both modes. At

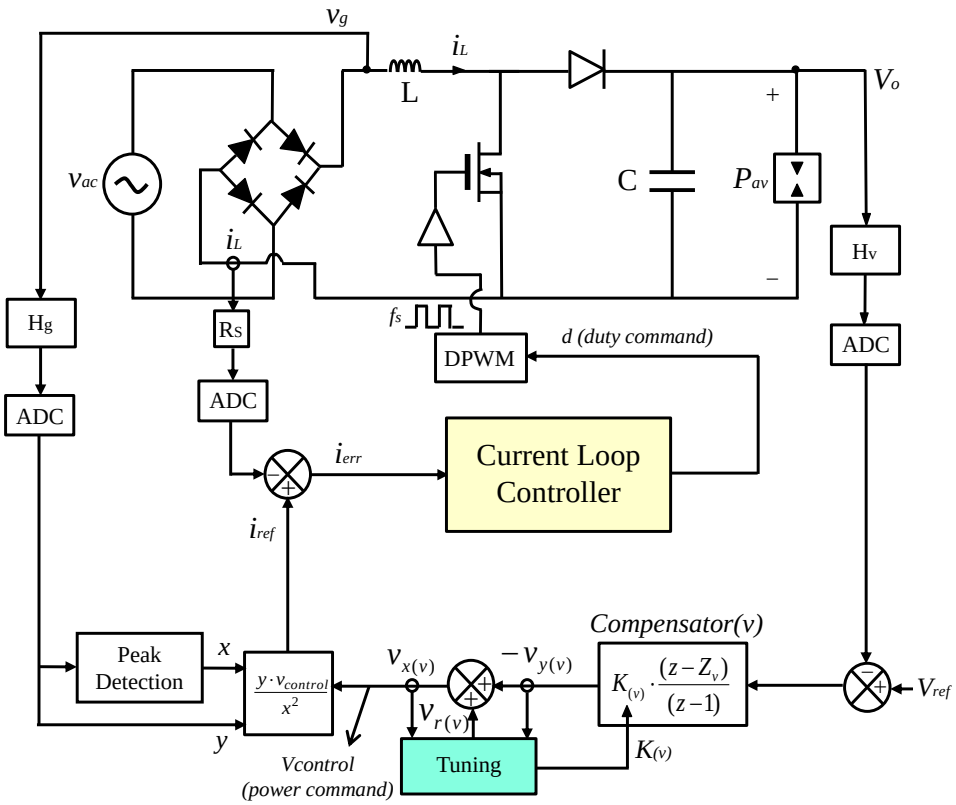


Fig. 6.1. Digitally controlled boost power factor correction (PFC) rectifier using average current-mode control with auto-tuning [8]

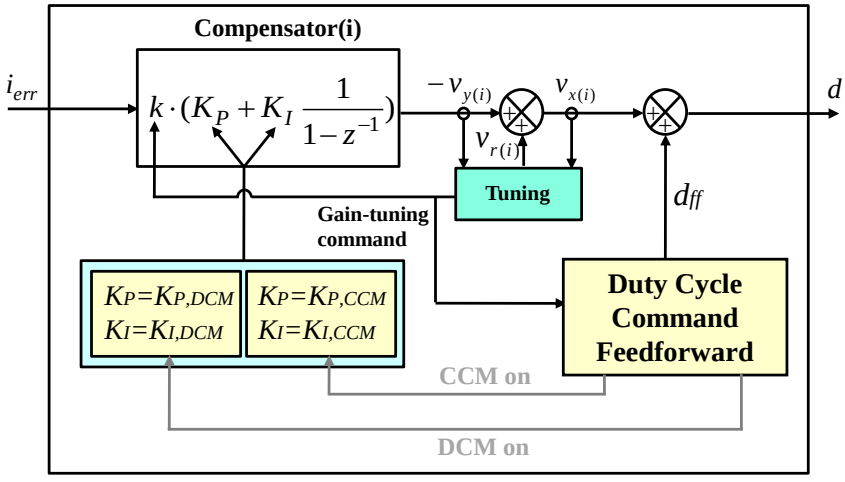


Fig. 6.2. Block diagram of the current loop controller with accurate mode boundary detection

intermediate loads, however, the system operates in DCM over a portion of the ac line period, and in CCM for the rest of the line period. In this mixed conduction mode (MCM), the controller should detect the operating mode and adjust the parameters appropriately. Unfortunately, even with such adaptive controller, undesirable transients may occur around the mode transitions due to abrupt changes in power stage dynamics. In order to deal with this issue, a duty cycle command feedforward technique has been introduced in [20]. The ideal duty cycle command values are calculated from the power stage and feedback loop parameters, consequently smoothing out the actual duty cycle command values during the mode transition transients. Furthermore, this duty cycle command feedforward technique is used for the mode boundary detection by calculating the intersection of CCM and DCM feedforward terms. However, all these approaches are based on the premise that the controller is capable of detecting the mode transition boundary precisely, which is difficult to accomplish in practice due to tolerances or uncertainties in the inductance value.

Various mode boundary detection methods have been reported in [35]-[37]. In [35], additional circuitry is employed in the controller to detect zero crossings of the inductor voltage. An expression based boundary detection using nominal L value is described in [36]. The mode boundary detection method presented in this chapter is based on auto-tuning and parameter estimation approach proposed in the previous chapter, in combination with the duty cycle command feedforward technique [38]. Fig. 6.1 shows a boost PFC rectifier with digital averaged current mode control

modified to include auto-tuning and boundary mode detection in the current control loop, as shown in Fig. 6.2.

The estimated L value, acquired by the current loop auto-tuning process, is used for the accurate mode boundary detection, such that the two-mode current loop compensator, which is designed separately for CCM and DCM to maintain the desired stability margins in both modes, switches its parameters according to the operating mode (CCM/DCM) determined by the boundary detection

This chapter is organized as follows. Section 6.1 introduces the DCM power stage dynamics and the auto-tuning effect on the DCM operation. Section 6.2 describes the duty cycle command feedforward technique. Application of these techniques to mode boundary detection in the current control loop is addressed in Section 6.3. Experimental results verifying the proposed approach are presented in Section 6.4, while Section 6.5 concludes the paper.

6.1 DCM dynamics and Auto-tuning Effect

To guarantee high performance of the system over wide load ranges, the first task is to find out DCM behavior of the system. In DCM, the power stage dynamics significantly different compared to that of CCM operation, and it is not investigated how auto-tuning compensator gain modulation method affects the DCM stability margins since it is conducted only in CCM. Tuners, in the current and voltage loops, monitor the signals before and after the perturbation injection point, and modify the compensator gains according to the pre-determined stability margins. Deviations of both current and voltage loop gains from the nominal operating points are dominated

by the tolerances of L and C respectively, and it has already been noted that the tolerances of L and C can be calculated from the tuning command k. Fortunately, in the current loop case, the power stage dynamics of CCM and DCM are found to be

$$G_{id\_ccm}(z) = \frac{\hat{i}_L}{\hat{d}} = \frac{V_o \cdot T_s}{L} \cdot \frac{1}{z-1} \tag{6.1}$$

$$G_{id\_dcm}(z) = \frac{\hat{i}_L}{\hat{d}} = \frac{v_g \cdot T_s}{2L} \cdot \frac{1}{z} \tag{6.2}$$

Since L is in the denominator in both cases, the tolerances of L shift the current loop gains by same degree in CCM and DCM. Now, it is apparent that the CCM tuning method, which simply modifies the compensator gain, also can be adopted for the DCM stability margin maintenance.

In designing the DCM compensator, simple I(integrator) compensator is enough, and input voltage v_g term can be removed by dividing it by itself. This will complex the hardware implementation though, it offers fixed stability margins. Consequently, the compensators for both CCM and DCM are represented as

$$\text{PI Compensator for CCM}: \quad G_{c\_ccm}(z) = K_{P\_ccm} + \frac{K_{I\_ccm}}{1-z^{-1}} \tag{6.3}$$

$$\text{Integrator for DCM}: \quad G_{c\_dcm}(z) = \frac{K_{I\_dcm}}{1-z^{-1}} \tag{6.4}$$

If the tuning command k is multiplied to K_{P_ccm}, K_{I_ccm}, and K_{I_dcm}, k only modifies the compensator gain in both CCM and DCM cases

$$G_{c\_ccm}(z) = k \cdot (K_{P\_ccm} + K_{I\_ccm}) \frac{(z - \frac{K_{I\_ccm}}{K_{P\_ccm} + K_{I\_ccm}})}{(z-1)} \tag{6.5}$$

$$G_{c\_dcm}(z) = k \cdot K_{I\_dcm} \frac{1}{1 - z^{-1}} = k \frac{K_{I\_dcm} \cdot z}{(z-1)} \tag{6.6}$$

Note that the nominal *k* value is 1. Final expressions for current loop gains for CCM and DCM are then

Current Loop Gain (CCM):

$$T_{i\_ccm}(z) = \frac{k}{L}(K_{P\_ccm} + K_{I\_ccm}) \cdot V_o T_s \cdot \frac{(z - \frac{K_{I\_ccm}}{K_{P\_ccm} + K_{I\_ccm}})}{(z-1)^2} \tag{6.7}$$

Current Loop Gain (DCM): $T_{i\_dcm}(z) = \frac{k}{L} \frac{T_s}{2} \frac{K_{I\_dcm}}{(z-1)}$ (6.8)

Both loop gains contain *k*/*L* term, which dramatically facilitates the tuning operation in CCM and DCM. Assume that *L* drifts +20% from the nominal value. Then, the tuner increases the tuning-command value *k* to 1.2, which cancels out the *L* tolerance effect in both CCM and DCM cases. As a result, only CCM tuning enables stability margins maintenance in both CCM and DCM.

6.2 Duty Cycle Command Feedforward

When the system is operating under nominal operating conditions, the ideal duty cycle command term can be calculated both in CCM and in DCM. If this feedforward term is applied to the current loop as shown in Fig 6.2, the current loop compensator has to compensate only for a small amount of deviation of the inductor current from the reference, which improves current shaping performance. Furthermore, when the system operates in MCM, the actual duty cycle command changes smoothly across the CCM/DCM boundary, without undesirable transients. In CCM, the duty

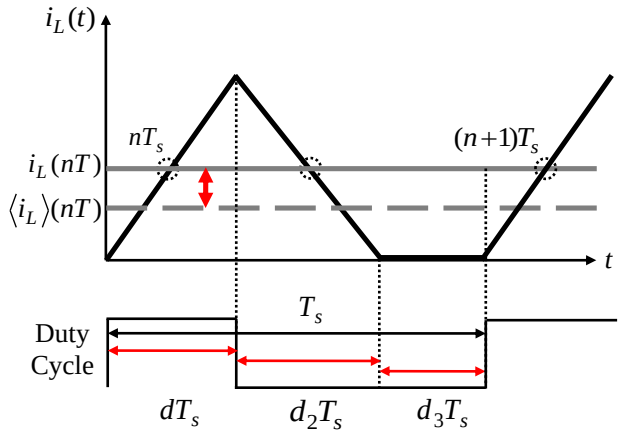


Fig. 6.3. Sampling correction in DCM

cycle command feedforward term $d_{ff,CCM}$ can be calculated from the ideal switch voltage, as a function of the rectified input voltage v_g and the output voltage V_o [20]:

$$d_{ff,CCM} = 1 - \frac{v_g}{V_o} \tag{6.9}$$

When the system is operating in DCM, the duty cycle command feedforward term is more complicated. In the digital average current mode control, current sampling is usually done at the midpoint of the transistor on time or the transistor off time, which in CCM corresponds to sampling the average inductor current. This is not the case in DCM, as illustrated by the waveform in Fig. 6.3, which shows that the difference between the sampled current and the average current increases as the converter operates deeper in DCM. To address this problem, a sampling correction factor can be applied [20], [23]. The same correction is applied here.

If the current loop controller works perfectly, the average current faithfully tracks the current loop reference $i_{reference}$ as

$$\left\langle i_L \right\rangle_{T_s} = i_{reference} = \frac{v_{control} \cdot v_g}{V_M{}^2 \cdot H_g} \tag{6.10}$$

where V_M represents the peak rectified input voltage. In Fig. 6.3, the average current can be calculated by finding the area under the inductor current waveform divided by the switching period,

$$\left\langle i_L \right\rangle_{T_s} = d \frac{v_g}{2L} \cdot (d + d_2) T_s \tag{6.11}$$

where the diode conduction duty cycle d_2 is

$$d_2 = \frac{v_g}{V_o - v_g} \cdot d \tag{6.12}$$

Applying (6.12) to (6.11), and equating (6.10) and (6.11) results in the ideal duty cycle command feedforward term in DCM:

$$d_{ff,DCM} = \sqrt{\frac{2L}{T_s} \cdot (\frac{v_{control}}{V_M{}^2 \cdot H_g})(1 - \frac{v_g}{V_o})} \tag{6.13}$$

The CCM and DCM duty cycle command feedforward terms are illustrated in Fig. 6.4 over one half ac line cycle, for several power levels. At high power, the converter is in CCM at all times and the CCM feedforward term (6.1) applies. At low power, the converter is in DCM and (6.13) applies at all times. At intermediate loads when the converter is in MCM, the intersection of CCM and DCM duty cycle command feedforward terms determines the mode boundary points, which can be acquired by equating (6.9) and (6.13),

$$d_{ff,CCM} = d_{ff,DCM} = 1 - \frac{v_g}{V_o} = \sqrt{\frac{2L}{T_s} \cdot (\frac{v_{control}}{V_M{}^2 \cdot H_g})(1 - \frac{v_g}{V_o})} \tag{6.14}$$

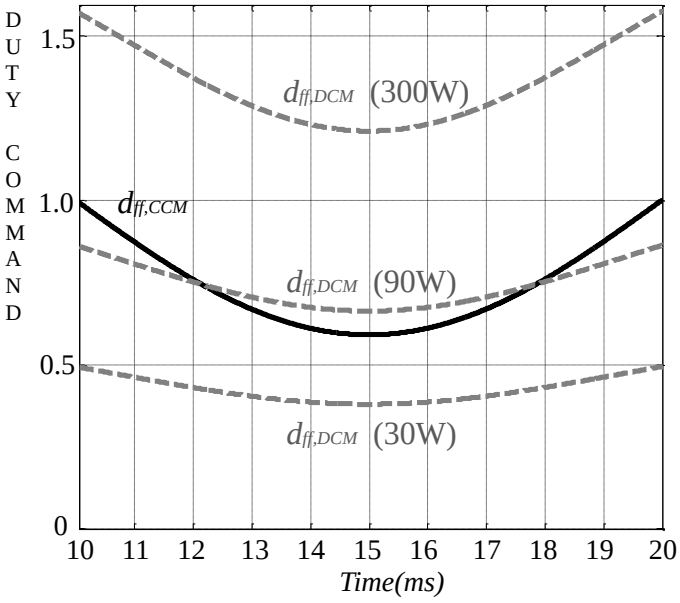


Fig. 6.4. Duty cycle command feedforward values for CCM and DCM for various output power (300 W (CCM):top, 90 W (MCM):middle, 30 W (DCM):bottom)

From (6.14), the CCM/DCM boundary occurs at the point when the rectified input voltage v_g crosses the value

$$v_g = (1 - \frac{2L}{T_s} \cdot (\frac{v_{control}}{V_M{}^2 \cdot H_g})) \cdot V_o \tag{6.15}$$

Equation (6.15) is used to determine the correct operating mode, and to employ the correct duty cycle command feedforward term, as well as the correct compensator parameters, as shown in Fig. 6.2, and discussed further in the next section.

6.3 Mode Boundary Detection and CCM/DCM Controller Realization

As discussed in Section III, the boundary detection is performed based on the CCM/DCM duty cycle command feed-forward term comparison. In MCM, the

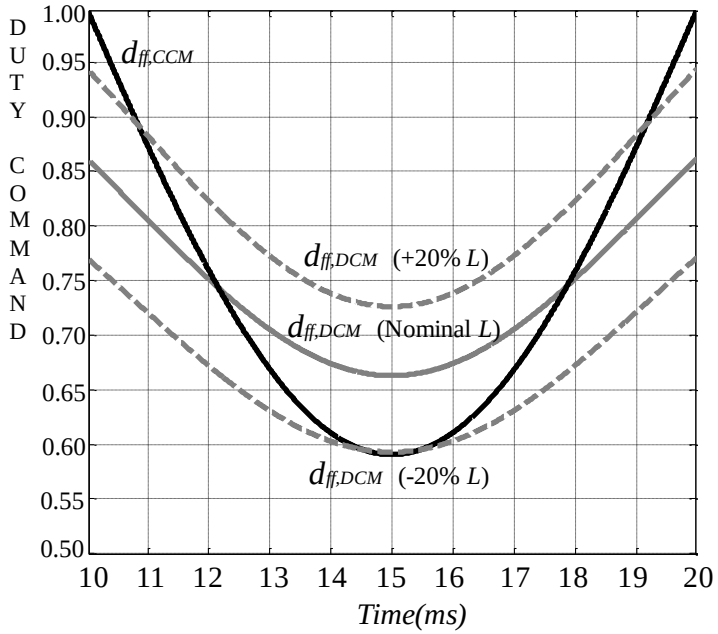
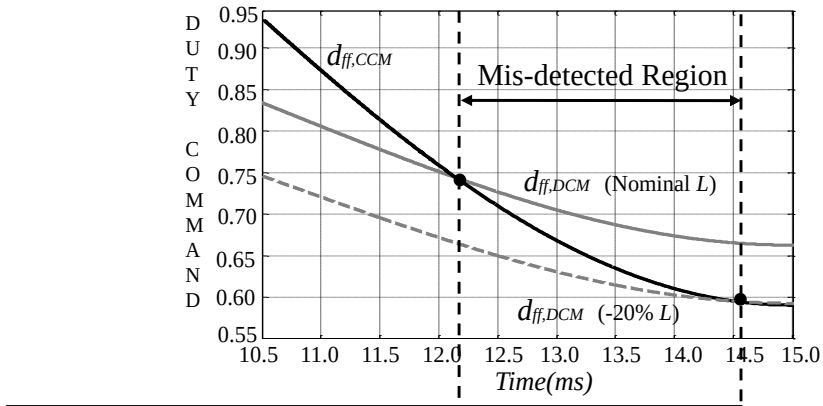


Fig. 6.5. Duty cycle command feedforward values for CCM (black) and DCM (grey) in the presence of ±20% L tolerances (upper dotted line:+20% L tolerance, middle solid line: nominal L, bottom dotted line: -20% L tolerance)

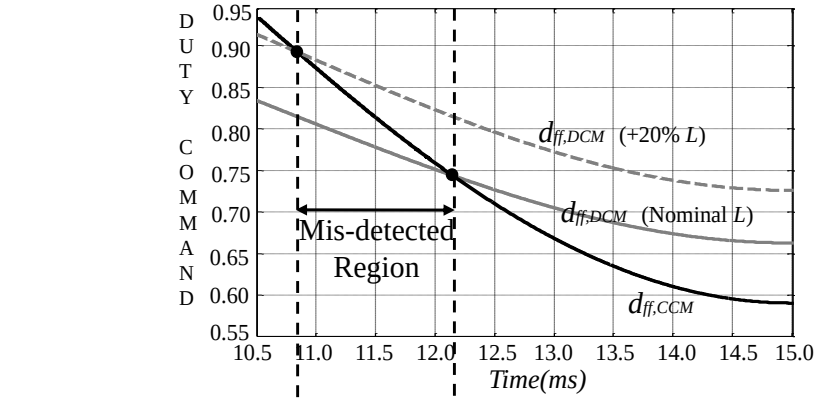
intersection of the two duty cycle command feed-forward terms determines the mode transition point as in (6.15), which is a function of L. With a conventional controller, the feedforward terms are computed based on the nominal L value, which implies errors in the presence of L tolerances or uncertainties as shown in Fig. 6.5. This boundary misdetection in turn causes erroneous controller operation for extended time interval called mis-detection region in Figs. 6.6 and 6.7.

In the proposed current loop controller, which is depicted in Fig. 6.2, the tuner produces the gain-tuning command (k) proportional to the actual inductance value. For example, +20% tolerance in L results in k = 1.2 gain-tuning command value. Thus, if the gain-tuning command k is multiplied by the nominal L_{nom} value in the boundary detection equation (6.15) as,



Actual Operating Mode	**DCM**	**DCM**
Detected Operating Mode	**DCM**	**CCM**

Fig. 6.6. Mis-detected region due to -20% L tolerance (CCM duty cycle command term (solid black), DCM duty cycle command with nominal L (solid grey), DCM duty cycle command with -20% L (dotted grey))



Actual Operating Mode	**CCM**	**CCM**
Detected Operating Mode	**DCM**	**CCM**

Fig. 6.7. Mis-detected region due to +20% L tolerance (CCM duty cycle command term (solid black), DCM duty cycle command with nominal L (solid grey), DCM duty cycle command with +20% L (dotted grey))

$$v_g = (1 - \frac{2L_{nom} \cdot k}{T_s} \cdot (\frac{v_{control}}{V_M{}^2 \cdot H_g})) \cdot V_o \quad (6.16)$$

the mode boundary is computed correctly even when the actual inductance value L differs from L_{nom}. Furthermore, the same gain-tuning command k multiplies L_{nom} in the DCM duty cycle feedforward term (6.13), thereby producing the corrected feedforward value in the presence of L tolerances. As a result, the duty cycle command feedforward block in Fig. 6.2 produces the correct duty cycle command feedforward value into the current feedback loop, and the correct compensator parameters are enabled based on the accurate mode boundary detection.

6.4 Experimental Results

A boost PFC rectifier is built with the following parameters $V_{g,rms}$ = 110 V, f_{line} = 50 Hz, V_o = 380 V, f_s = 100 kHz, L_{nom} = 0.5 mH, C = 220 μF, to verify the performance of the proposed approach. Digital controller was Verilog-HDL coded and implemented on a Xilinx Virtex-IV FPGA.

In CCM, the current control loop is designed to have 10 kHz bandwidth and 55° phase margin, and the voltage loop is designed to have 5 Hz bandwidth and 68° phase margin. For both loops, simple proportional-integral (PI) compensators are implemented. When the system goes into DCM, the CCM compensator for the current loop is disabled, and the simple integral (I) DCM compensator is activated so that the current loop has 5 kHz bandwidth with 90° phase margin.

The current loop auto tuner injects digitally generated sinusoidal perturbation signal oscillating at the nominal crossover frequency (10 kHz), which is the nominal

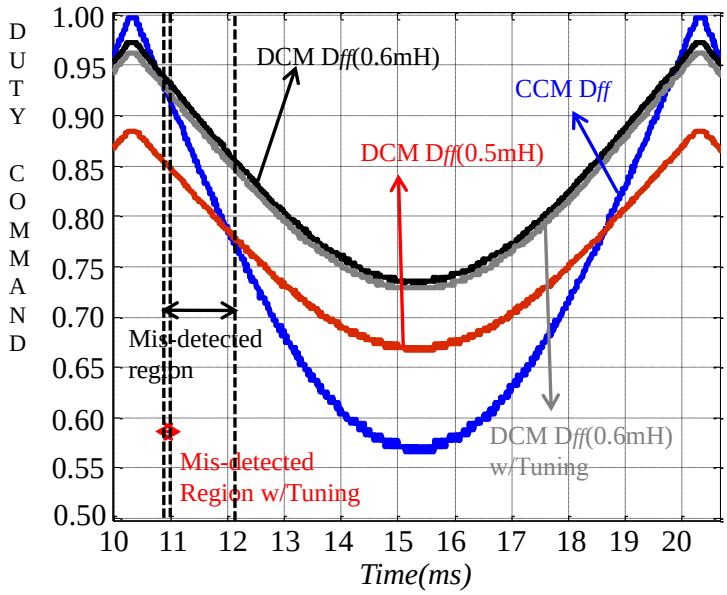


Fig. 6.8. Duty cycle command (D_{ff}) values for CCM and DCM in the presence of +20% L tolerance and boundary mis-detected region at P_{load} = 90 W. (CCM duty cycle command: DCM duty cycle command with L_{nom} = 0.5 mH : DCM duty cycle command with L = 0.6 mH (black): adjusted DCM duty cycle commands with L = 0.6 mH after tuning (grey))

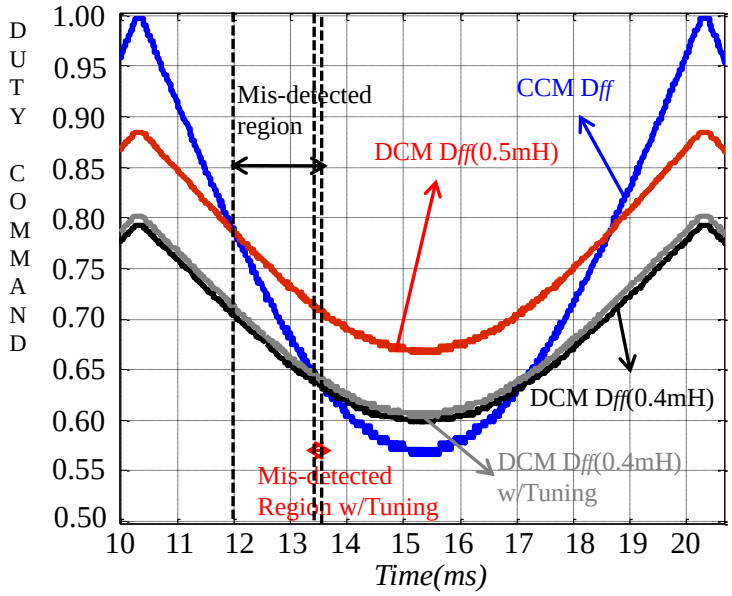


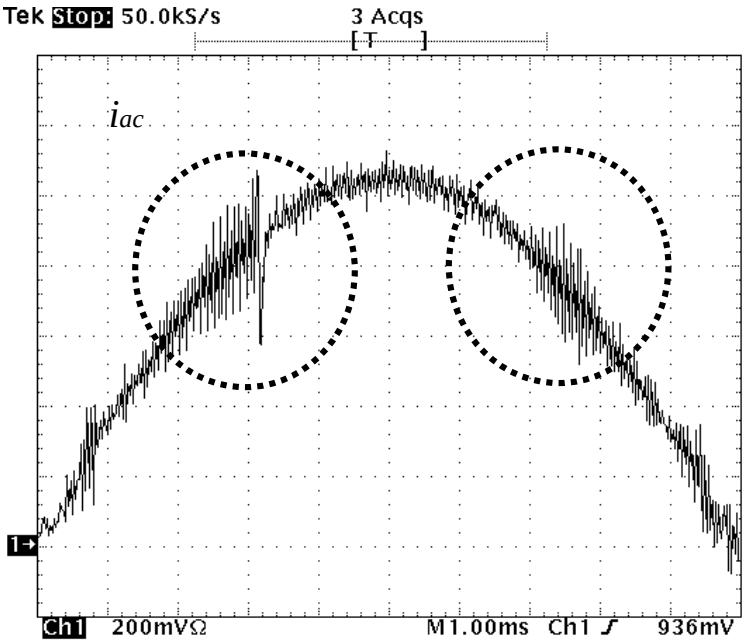
Fig. 6.9. Duty cycle command (D_{ff}) values for CCM and DCM in the presence of -20% L tolerance and boundary mis-detected region at P_{load} = 90 W. (CCM duty cycle command: DCM duty cycle command with L_{nom} = 0.5 mH: DCM duty cycle command with L = 0.4 mH (black): adjusted DCM duty cycle command with L = 0.4 mH after tuning (grey))

Table 6.1: Actual Inductance vs Estimated inductance

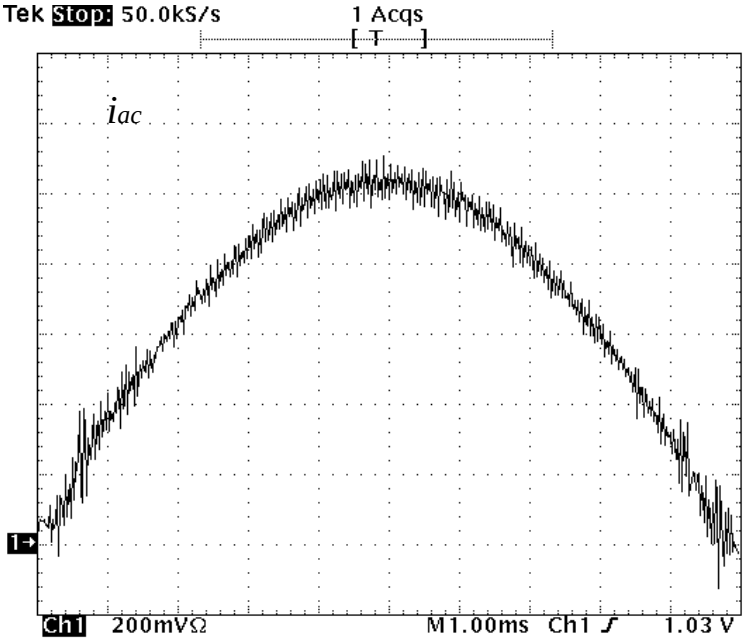
Actual Inductance	Actual Tolerance	Estimated Inductance	Estimated Tolerance	Estimation Error	Tuning Command (k)
0.400mH	-20%	0.411mH	-17.8%	2.75%	0.822
0.450mH	-10%	0.458mH	-8.4%	1.78%	0.916
0.485mH	-3%	0.491mH	-1.9%	1.24%	0.981
0.515mH	+3%	0.511mH	+2.1%	0.78%	1.021
0.550mH	+10%	0.552mH	+10.3%	0.36%	1.103
0.600mH	+20%	0.594mH	+18.7%	1.00%	1.187

current loop crossover frequency in CCM. This perturbation signal (10 kHz) is based on 10 samples per switching period.

Figs. 6.8 and 6.9 show how precisely the tuner can estimate the tolerance of L and correctly determine the mode boundaries. The datapoints are retrieved using Xilinx Chipscope 9.2. Tests are performed with L having the nominal value, as well as +20% and -20% tolerance with respect to the nominal value. First, the tuner is activated at full load (300 W) to acquire the L value, and then the system is operated at an intermediate load of 90 W. In Figs. 6.8 and 6.9, each curve in the middle represents the ideal CCM and DCM duty cycle commands when the inductance has the nominal value of 0.5 mH. The ideal DCM duty cycle commands with 0.6 mH, and 0.4 mH inductances, which represent ±20% inductance tolerances, are also shown. After tuning, the computed DCM feedforward terms by the controller (light grey curves), approach the desired values (dark black curves). Consequently, the mis-detected regions are minimized in both cases. The tolerance prediction capability of the tuning module is also summarized in Table 6.1. For various tolerances, the tuner estimates the actual inductance with good accuracy.

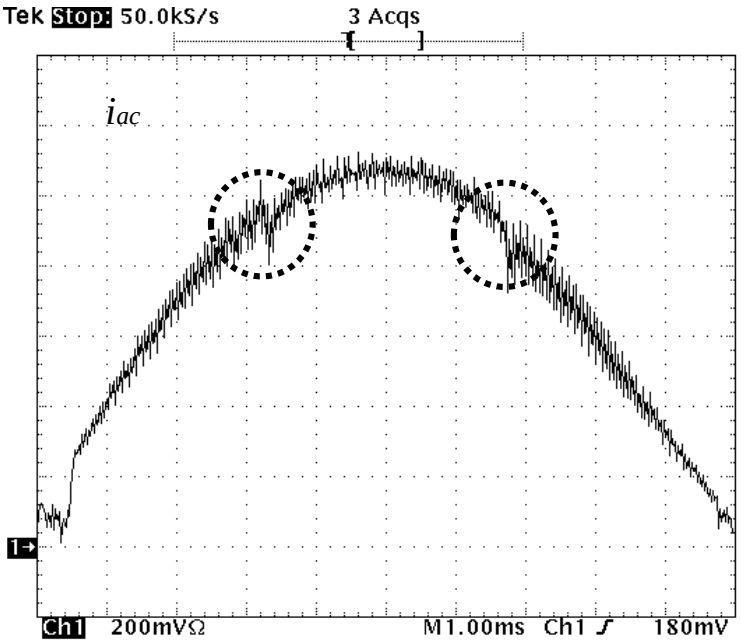


(a)

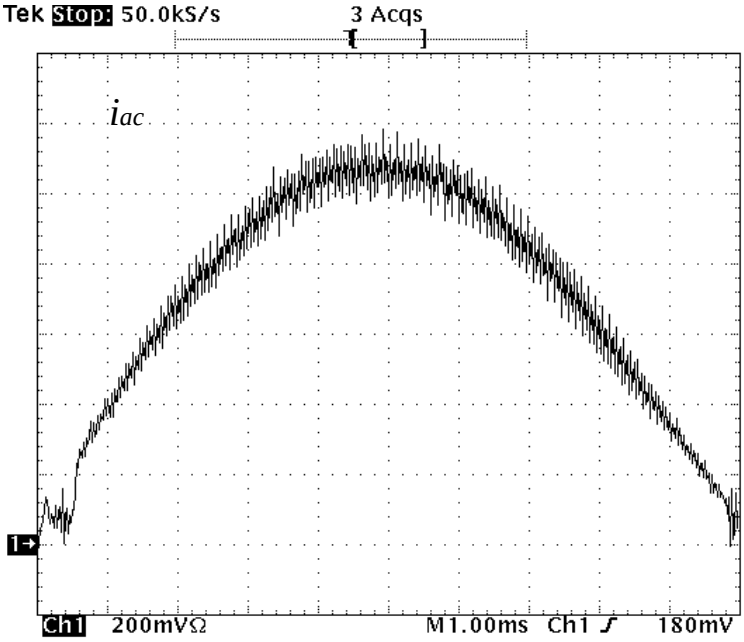


(b)

Fig. 6.10. Input current waveforms (a) AC line current i_{ac} with +20% inductor tolerance (before tuning), (b) AC line current i_{ac} with +20% inductor tolerance (after tuning). ch1: 200 mA/Div, time: 1 ms/Div. P_{load} = 75 W, V_g=110V_{rms}, f_{line}=50Hz



(a)



(b)

Fig. 6.11. Input current waveforms (a) AC line current i_{ac} with -20% inductor tolerance (before tuning), (b) AC line current i_{ac} with -20% inductor tolerance (after tuning). ch1: 200 mA/Div, time: 1 ms/Div. P_{load} = 75 W, V_g=110V_{rms}, f_{line}=50Hz

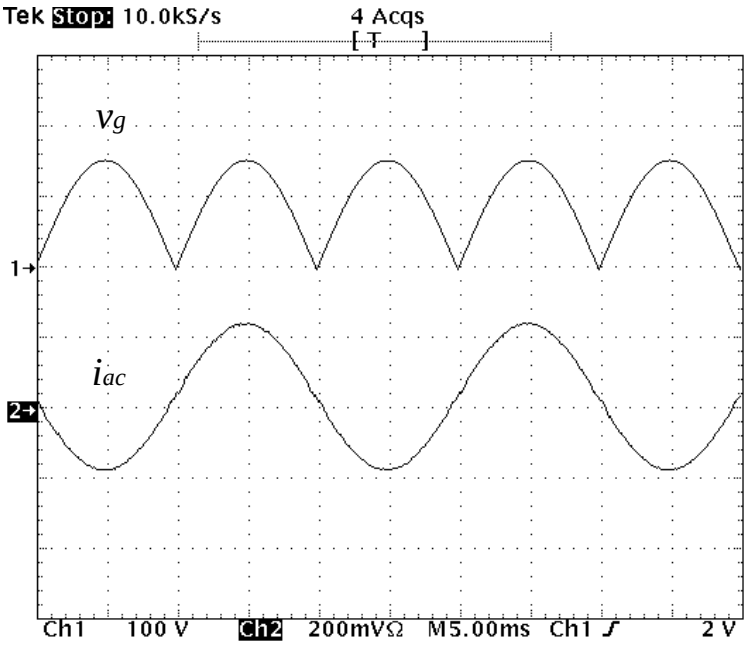


Fig. 6.12. Post-tuning rectified input voltage and input current waveforms, ch1: Rectified input voltage (v_g)- 100 V/Div, time: 5 ms/Div, ch2: AC line current (i_{ac})- 200 mA/Div, time: 5 ms/Div. P_{load} = 75 W, V_g=110V_{rms}, f_{line}=50Hz

The input current distortion due to the conduction mode mis-detection is shown in Figs. 6.10 and 6.11. In Fig. 6.10, in the presence of +20% tolerance, the controller recognizes the mis-detected region as DCM, while it is operating in CCM. In this case, DCM integral (I) compensator, which is not suitable for CCM in terms of phase margin, is applied to the system operating in CCM. As a result, unstable behavior occurs in this mis-detected region as shown in Fig. 6.10(a). After tuning, since this mis-detected region is minimized by taking into account the *L* tolerance effect, the un-desirable ripple disappears. In the case of -20% tolerance, the CCM PI compensator is applied to the converter operating in DCM during the mis-detected region. Although instability does not occur in his case, the bandwidth of the control loop is reduced,

Table 6.2: Hardware Requirements

	Logic Gates
Digital Average Current Mode Controller	4499
Current Loop Tuning Module	4615
Voltage Loop Tuning Module	3612
Boundary Detection Module (w/ Duty cycle command feed-forward)	3804

resulting in a slight increase in distortion, as shown in Fig. 6.11(a). After tuning, this small transient at the transition boundary is removed. Fig. 6.12 shows the final post-tuning system operation, which exhibits 3.4% input current THD and 0.999 power factor (PF) at 75 W output power. The hardware requirements for both current and voltage tuning modules as well as boundary detection module are specified in Table 6.2.

From equations (6.9), (6.13), and (6.14), the switching period T_s and the output voltage V_o are constants, and only multiplications by f_s or $1/V_o$ are performed. The hardware required for the calculation of the term ($v_{control}/V_M^2 \cdot H_g$) is included in the 4,499 gates of the Digital Average Current Mode Controller, as reported in Table 6.2, and includes one digital divider. As for the square root calculation, it is performed using Virtex IV built-in square root core generator, which occupies most part of the Boundary Detection Module (approximately 2800 gates). Overall, the Boundary Detection Module computes few multiplications and one square root. The total gate number 3,804 reported in Table 6.2 therefore includes all the hardware in the Boundary Detection Module, with the square-root calculation.

The experimental results verify the performances of the tuning module at different operating conditions and against tolerances in the filter components with negligible perturbation effects on the system during tuning operation as well as accurate mode boundary detection, and high-performance current shaping in MCM without the need for advance knowledge of the inductance value.

6.5 Conclusions and Discussion

This chapter presents an accurate conduction mode boundary detection method, which is performed based on the auto-tuning and parameter estimation approach proposed in the previous chapter, in combination with the duty cycle command feedforward technique. The proposed approach does not require prior knowledge of L or C and results in robust auto-tuning of the control loops as well as accurate mode boundary detection. Experimental results on a 300 W digitally controlled single-phase boost power factor correction rectifier verify operation of the proposed technique in the presence of wide inductance tolerances.

CHAPTER 7

Auto-tuning of Digitally Controlled Grid-tied DC-AC Inverters

A DC-AC inverter converts DC power from a resource such as photovoltaic modules into AC power to be compatible with the residential load or the AC grid [38]-[50]. The DC power produced by a PV array is maximized by peak power tracking technique (MPPT), and converted into alternating (AC) power by the following DC-AC power conversion stage.

In the PV system, power imbalance between PV power and the residential power consumption is inevitable. Depending on how this imbalance is dealt with, the DC-AC inverter can be classified into two different types. A stand alone (SA) type DC-AC inverter system independently operates and connected to the residential loads, but not to the AC grid. Thus, in order to balance the power between the source and the load, an energy storage unit (e.g. a battery system) is required [41].

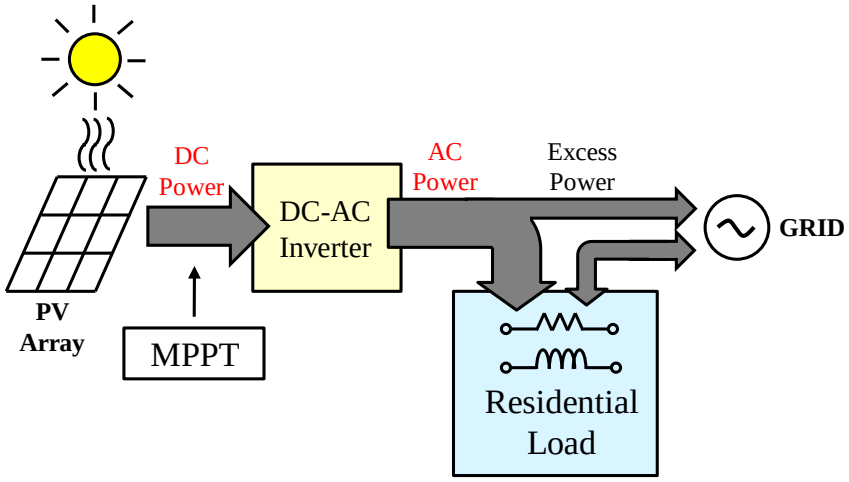


Fig. 7.1. Grid-tied PV power system

The grid-tied type inverter system, on the other hand, is tied to the grid in parallel, thus resolving the power imbalance between the PV source and the residential load. For instance, when the PV array produces more power than what is consumed by the residential load, the excess energy can be sold to the grid. In the opposite case, when the energy produced by the PV system is less than needed, the loads can be supplied by the grid, as shown in Fig. 7.1. Therefore, in order to maximize the usable energy supplied to the residential load or sold to the grid in grid-tied inverter system, it is desired to achieve purely active grid power, which is possible by accomplishing unity power factor. Moreover, since the DC-AC inverter is located at the end point to deliver the AC power to the grid, the quality of the grid current is specified by the tight standard IEEE 1547 because these systems are viewed as sources as opposed to the AC-DC rectifier systems, which are considered as loads. The standard specifies the maximum

Table 7.1: Maximum harmonic current distortion in percent of current (I_{grid})

Indivisual harmonic order h (odd harmonics)	h<11	11≤h<17	17≤h<23	23≤h<35	35≤h	Total demand distortion (TDD)
Percent (%)	4.0	2.0	1.5	0.6	0.3	5.0

permissible individual harmonic content in the grid current, as well as total demand distortion (TDD), which has to be less than 5% as shown in Table 7.1 [51].

Similar to the AC-DC rectifier (PFC) system, the power stage filter component tolerances modify the DC-AC inverter system dynamics. The system stability and the power factor can be degraded due to this unexpected filter component value variations. Consequently, the effectiveness of the power transfer from the PV source to the residential load or grid can be affected. Hence, it is required to maintain stable system operation against any undesired power stage passive component tolerance disturbances or other uncertainties.

In Section 7.1, the inverter system behavior and the characteristics are investigated in order to explore the possibility of applying the tuning technique developed in Chapters 5 and 6 for AC-DC rectifiers. Section 7.2 analyzes the power stage dynamics and compares the results to the AC-DC rectifier system to support the concept assumed in the previous section. Detailed control loop design and MATLAB simulation results are given in Section 7.3. The hardware realization is described in Section 7.4, while experimental evidence validating the proposed concept is presented in Section 7.5. Section 7.6 concludes the chapter.

7.1 Grid-tied Inverter and boost PFC system

The complete DC-AC inverter circuitry is shown in Fig. 7.2. The power produced by PV array is modeled as a power source. Energy storage capacitor is located next to the PV array to maintain the power level. The DC-DC buck stage scales the PV voltage down to the appropriate level. A slow unfolder converts the DC power into AC power [40], [41]. In order to achieve unity power factor, shaping the inductor current in phase and identical shape as rectified grid voltage takes priority over the other system objectives. The system analysis starts from the fact that the grid-tied DC-AC system shows power stage characteristics similar to the AC-DC PFC rectifier system. When the grid-tied DC-AC inverter system is seen from the grid

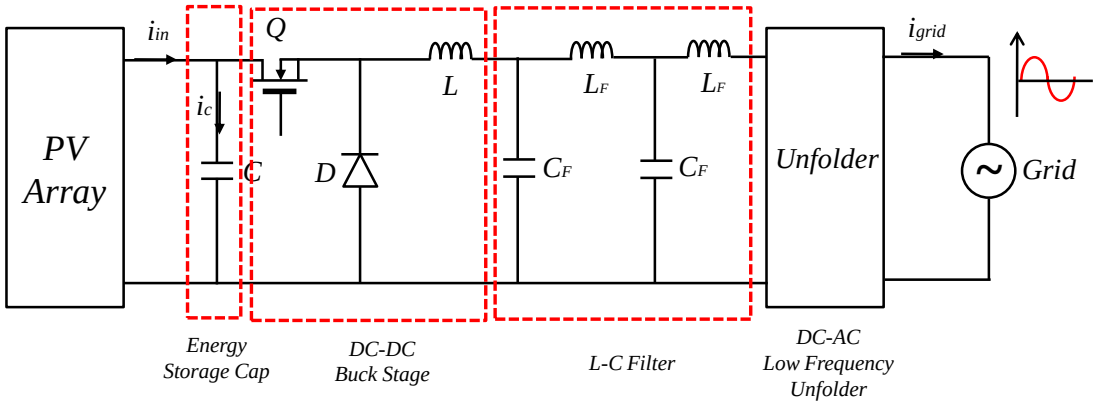


Fig. 7.2. Grid-tied DC-AC Inverter

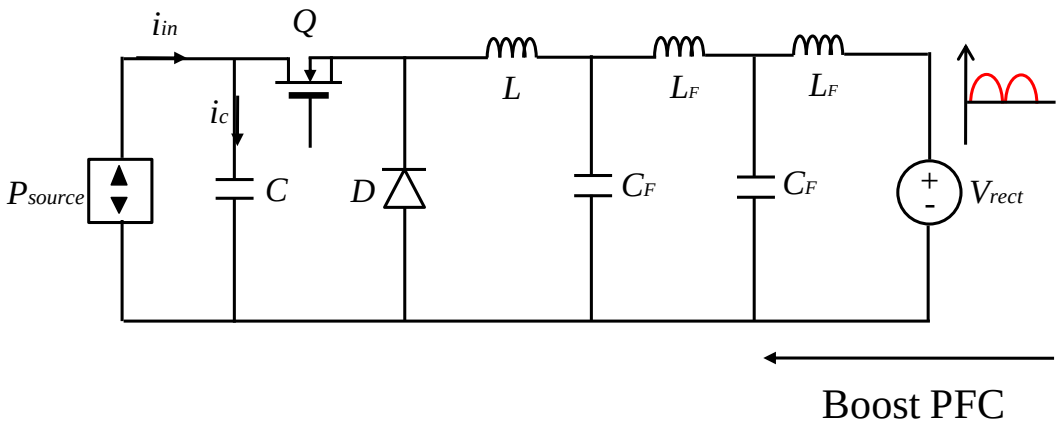


Fig. 7.3. Simplified Grid-tied DC-AC Inverter

side, it has very similar structure as the boost PFC (Power Factor Correction) rectifier stage. In other words, this grid-tied DC-AC inverter system can be controlled in a very similar manner as the boost PFC system.

If the PV output power is assumed to be controlled to produce the peak power (MPPT), and the grid voltage after the low-frequency (50~60 Hz) unfolder is purely sinusoidal, then the circuit schematic can be further simplified as shown in Fig. 7.3. The PV array output power is modeled as a power source, and the output voltage is rectified sinusoidal wave. In this case, looking from the rectified AC source backward, the buck power stage can be seen as a boost stage with the MOSFET and the diode locations swapped and the current flow reversed. Thus, if the MOSFET switch is controlled in the same way the diode operates in a boost PFC rectifiers, the system shows identical power stage dynamics (the duty command variation to the inductor current variation) as the AC-DC rectifier system. The duty command (d) for the buck stage is exactly the same as the diode turn on ratio (1-d) in the boost PFC system. This implies that digital average current mode control technique can be used in such a way

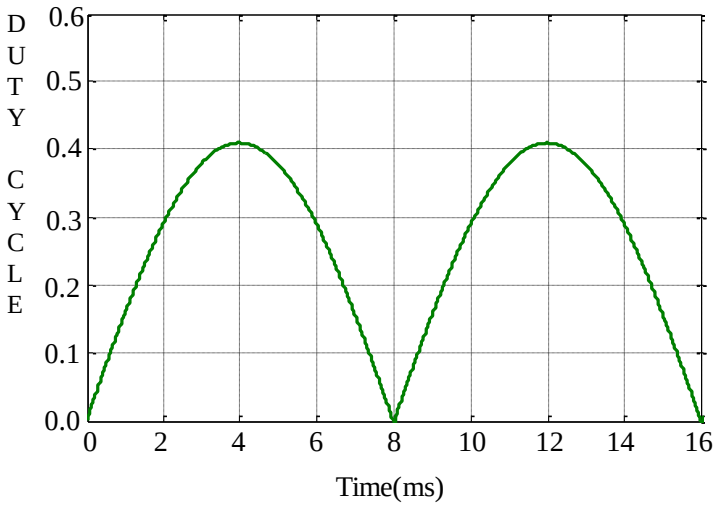


Fig. 7.4. Duty Cycle Command

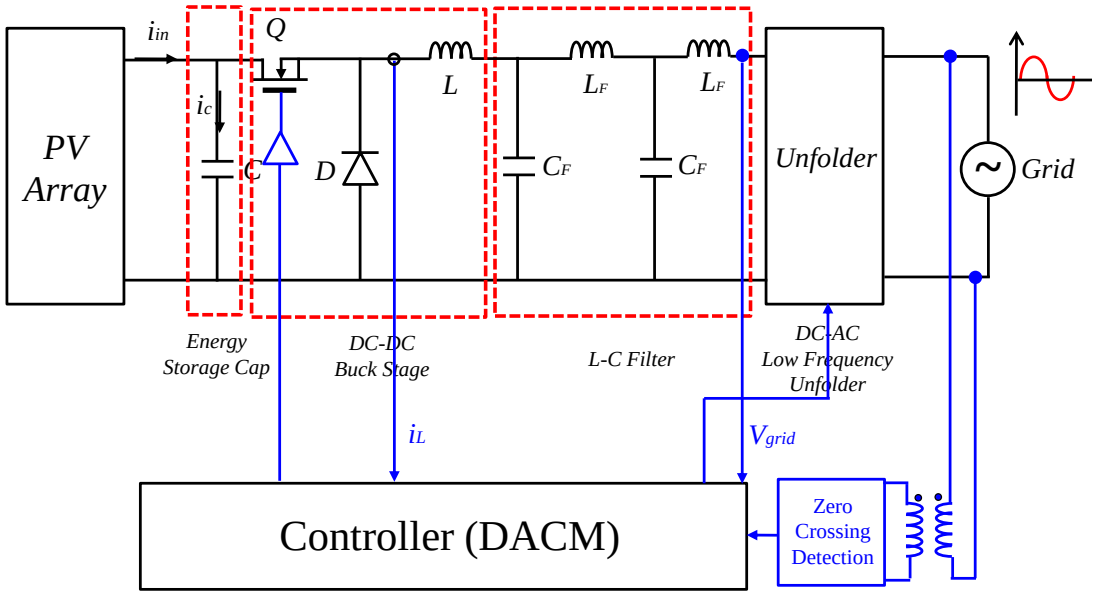


Fig. 7.5. Digital Average Current Mode Controlled Grid-tied DC-AC Inverter

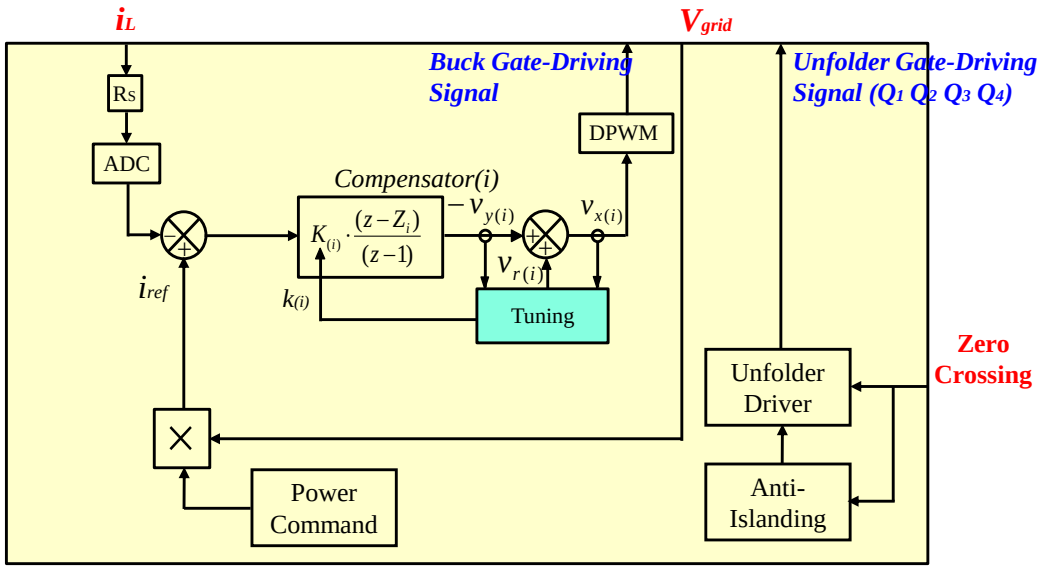


Fig. 7.6. Detailed digital controller implementation

that the controller produces the MOSFET switch turn-on duty ratio as (1-*d*), which is the diode turn on time of the boost PFC rectifier. This conclusion is validated by the simulation result illustrated in Fig. 7.4, and the power stage modeling in the next section. In Fig. 7.4, it is easy to see that the duty cycle command is exactly 1-*d* (diode turn on ratio) of PFC rectifier system. The full DC-AC inverter schematic employing the digital average current mode control technique is shown in Fig. 7.5.

The grid voltage zero crossing detection is conducted by additional isolated circuitry. Simple anti-islanding is performed by measuring the frequency of the grid voltage. The controller continuously monitors the zero crossings of the grid voltage, and shuts down all the unfolder switches when the frequency is out of a pre-set tolerance range.

The tuning module is implemented after the current compensator to inject the perturbation and manipulate the compensator gain. The detailed controller block diagram is shown in Fig. 7.6. Based on the digital average current mode controller, the slow unfolder driving module and the tuning module are added.

7.2 Power Stage Dynamics

The power stage transfer function from the duty cycle command to the inductor current can be derived in a very similar way as in the PFC system [6]. From the large signal averaged model in Fig. 7.7, the averaged inductor voltage equation over one switching period can be constructed as

$$L\frac{d\langle i_L\rangle_{T_s}}{dt} = d(t)\cdot\langle V_{pv}\rangle_{T_s} - \langle V_{rect}\rangle_{T_s} \tag{7.1}$$

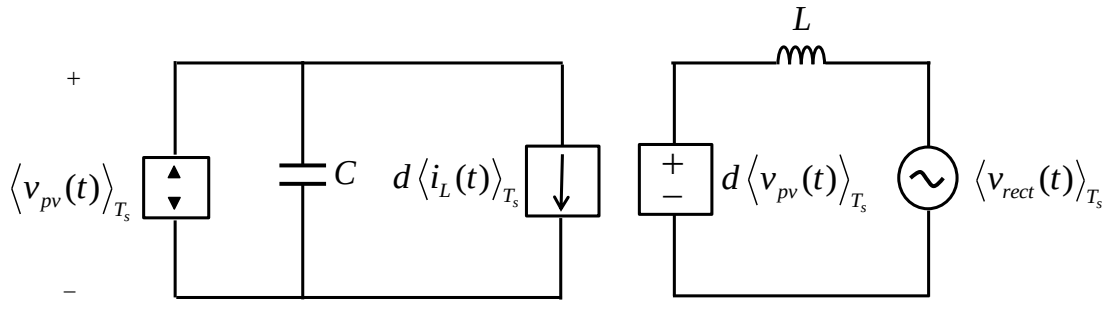


Fig 7.7. Large signal model averaged over switching period T_s

where V_{pv} is the PV array voltage, and V_{rect} is the rectified grid voltage. When it is assumed that PV voltage variation is much smaller that the large signal input voltage as in (7.2),(7.3),

$$\left\langle v_{pv} \right\rangle_{T_s} = V_{pv} - \hat{v}_{pv}(t) \tag{7.2}$$

$$\left| \hat{v}_{pv} \right| << \left| V_{pv} \right| \tag{7.3}$$

The small-signal equation becomes

$$L\frac{d\left\langle i_L \right\rangle_{T_s}}{dt} = d(t)(V_{pv} - \hat{v}_{pv}) - \left\langle V_{rect} \right\rangle_{T_s}$$

$$= d(t)V_{pv} - \left\langle V_{rect} \right\rangle_{T_s} \tag{7.4}$$

If the switching frequency (~100kHz) is much higher than the grid frequency (50~60Hz), the rectified grid voltage can be considered to be constant over one switching period. The averaged duty-to-inductor current transfer function can then be obtained by assuming the rectified grid voltage is constant, and taking Laplace transform of each term.

$$G_{id}(s) = \frac{i_L(s)}{d(s)} = \frac{V_{pv}}{sL} \tag{7.5}$$

(7.5) is consistent with the PFC system power stage dynamics. The magnitude response of (7.5) scales up and down with tolerance in L. Therefore, auto-tuning technique developed in Chapters 5 and 6 for the PFC system can also be employed in DC-AC inverter system. This is further verified by MATLAB simulations and by experimental results.

7.3 Control Loop Design Example and Simulation Verification

From Section 7.2, it is confirmed that the current loop power stage dynamics show identical behavior as the AC-DC rectifier system. Since the objective is to develop a discrete-time power stage model, which is needed for digital control system design, the power stage control-to-inductor current transfer function obtained from the discrete-time small signal modeling in Section 4.2.1 is

$$G_{id}(z) = \frac{V_{pv}}{L} \cdot \frac{T_s}{z-1} \quad , \tag{7.6}$$

and the entire current loop gain expression becomes

$$T_i(z) = G_{id}(z) \cdot G_{ci}(z) \cdot G_{DPWM}(z) \cdot R_s \tag{7.7}$$

where $T_i(z)$ is the inverter current loop gain, $G_{ci}(z)$ is the current loop compensator, $G_{DPWM}(z)$ is the DPWM transfer function, and R_s is the inductor current sensing gain.

The controller is designed based on the following power stage parameters V_{pv}= 300 V, f_{line}= 50 Hz, V_{grid}= 110 V_{rms}, f_s=100 kHz, L=0.4 mH, C= 330 μF, P_{av}=120 W. The power stage control-to-inductor current transfer function obtained from the discrete-time small signal modeling from (7.6) becomes

$$G_{id}(z) = 7.5 \frac{1}{z-1} \tag{7.8}$$

The PI current loop compensator is sufficient to achieve specific stability margins f_c= 10 kHz, φ_m= 55° similar to the AC-DC rectifier case,

$$G_{ci}(z) = 0.0693 + \frac{0.0154}{(1-z^{-1})} \tag{7.9}$$

Magnitude and phase Bode plots for the inner current loop gain are illustrated in Fig. 7.8.

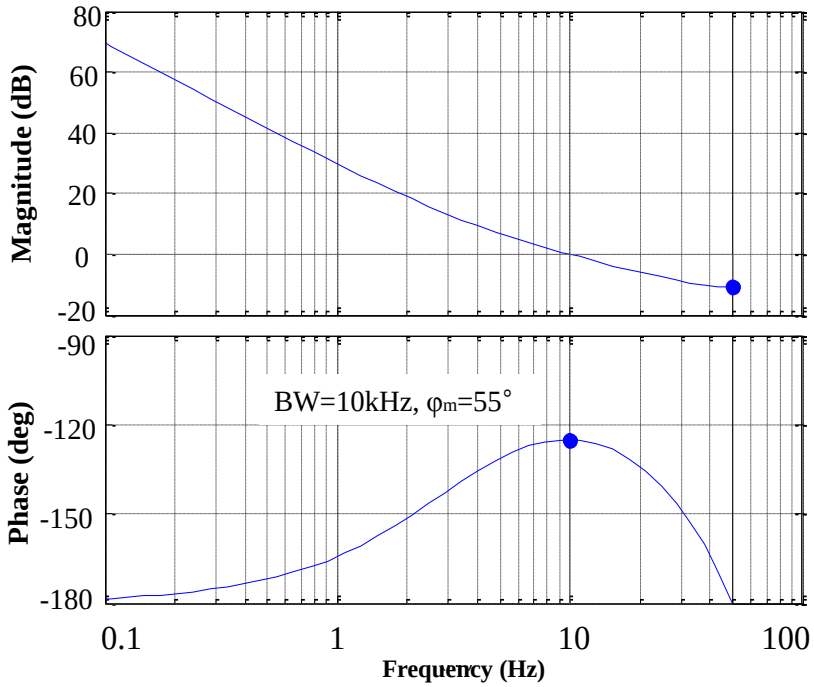
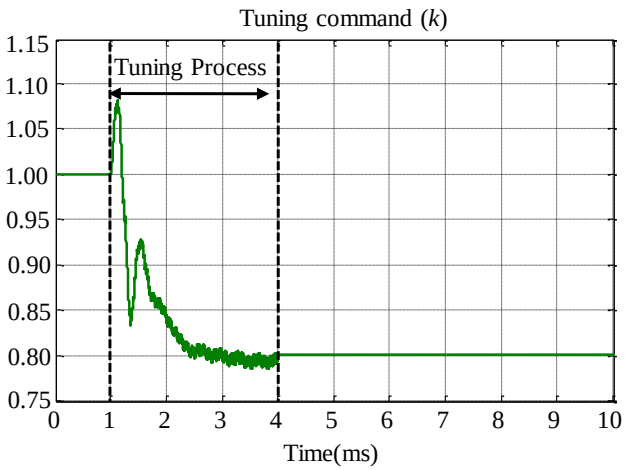


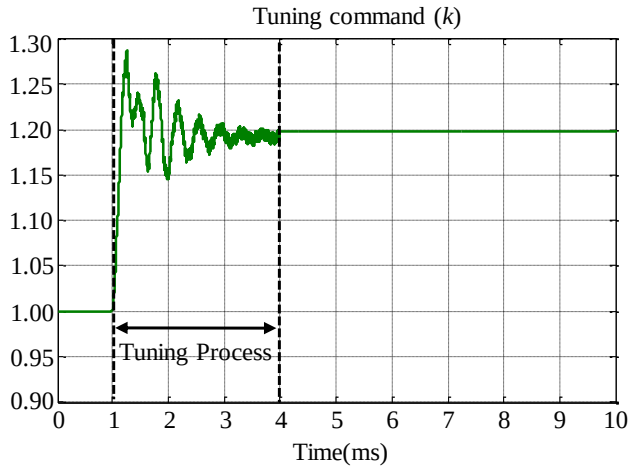
Fig. 7.8. The current loop gain bode diagram

Using a MATLAB/Simulink model, it is verified that the power stage modeling is correct, and the auto-tuning technique is compatible with the grid-tied inverter system. It is assumed that the inductance has tolerance spanning ±20% of the nominal value (500μH). In extreme cases (at +20% and -20% tolerance), the tuning is activated and the desired tuning behavior is observed. Fig. 7.9 shows the case of -20% inductance tolerance. The tuning command settles down to 0.8, which indicates -20% tolerance. The +20% tolerance case in shown in Fig. 7.10. The tuning command converges to 1.2, which implies +20% tolerance.



-20% tolerance (L=0.4mH)

Fig 7.9. Tuning Command (-20% *L* tolerance)



+20% tolerance (L=0.6mH)

Fig 7.10. Tuning Command (+20% *L* tolerance)

7.4 Hardware Realization

The digital controller for the experimental prototype was implemented on Virtex-IV FGPA development platform, and the target power stage set-up is shown in Fig. 7.11. The controller controls the DC-DC stage switch based on the digital average current mode control technique. The unfolder, which flips the DC power into AC power is controlled by detecting the zero crossings of the grid voltage using additional circuitry. Inductor current and the rectified grid voltage are sampled at the middle of falling edges of the inductor current so that the controller has enough time to produce duty cycles close to 0. With the rising edge sampling, it is not possible to produce the duty cycle less than 5% due to the A/D converter delay, and the controller computing time. The detailed zero crossing circuitry is described in Fig 7.12. The grid

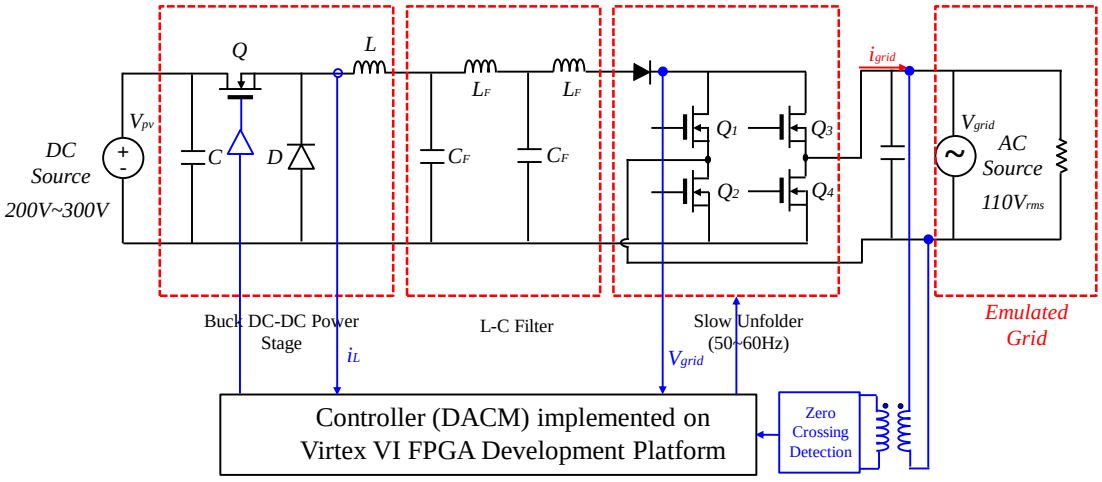


Fig. 7.11. Experimental set-up

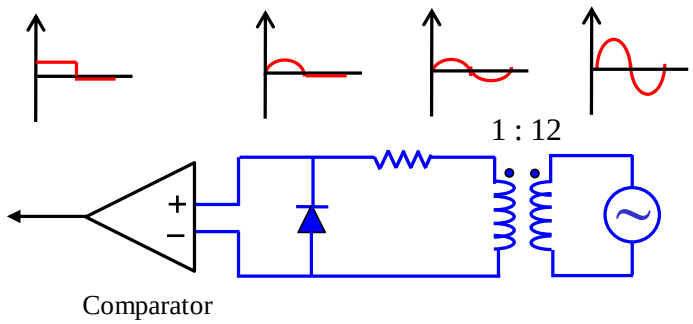


Fig 7.12. Zero crossing detection

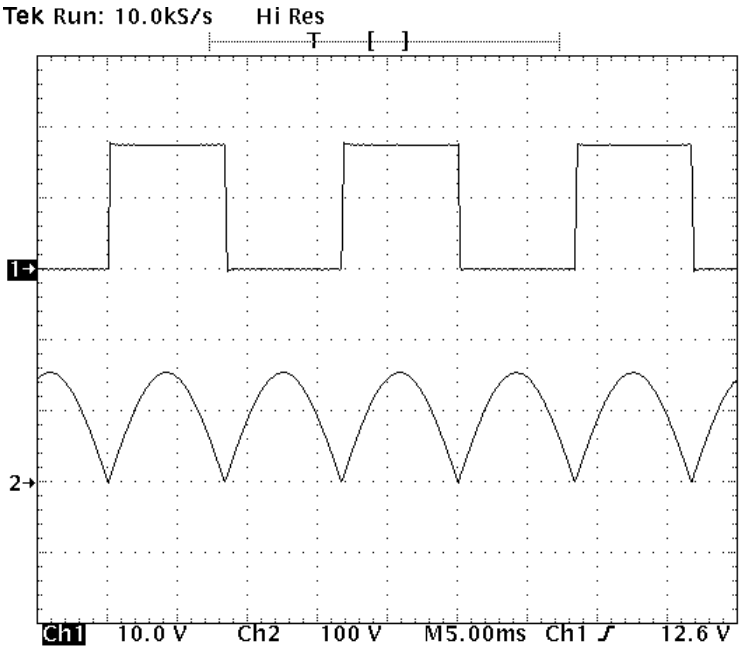


Fig 7.13. Zero crossing detection waveform
Ch 1: Zero crossing detection signal : 10V/DIV, Ch 2: Rectified grid voltage : 100V/DIV

voltage is isolated and scaled using 12:1 transformer, and the clamp diode and the comparator produce the zero crossing signal.

Undesirable ripples at both edges of the zero crossing pulses are compensated in the controller as required to drive the unfolder switches in a stable manner. Fig. 7.13 shows the zero crossing detection signal and rectified grid voltage resulted from proper unfolding behavior.

7.5 Experimental Results

Grid-tied DC-AC inverter system is analyzed, and compatibility of the tuning technique has been verified using MATLAB/Simulink model. Experimental verification is presented in this section.

The experimental set-up is shown in Fig 7.11. The main differences from the target set-up from Fig 7.5 are the power source and the grid. The power source is implemented with a high-voltage DC source, and the grid part is emulated by a combination of AC source and a resistor. The current flows to the emulated grid is considered as grid current i_{grid}.

The power stage parameters and the stability margins are as follows: input DC voltage = 300 V, AC Grid voltage = 110 V_{rms}, Power = 120 W, L= 400 μH, C= 330 μF, f_{line} = 60 Hz, f_s = 100 kHz, Stability Margins: φ_m = 55°, f_c= 10 kHz.

Under the nominal operating condition, the stable system operation is shown in Fig. 7.14. The rectified grid voltage and the grid current are in shape, therefore resulting in high power factor and low current harmonics.

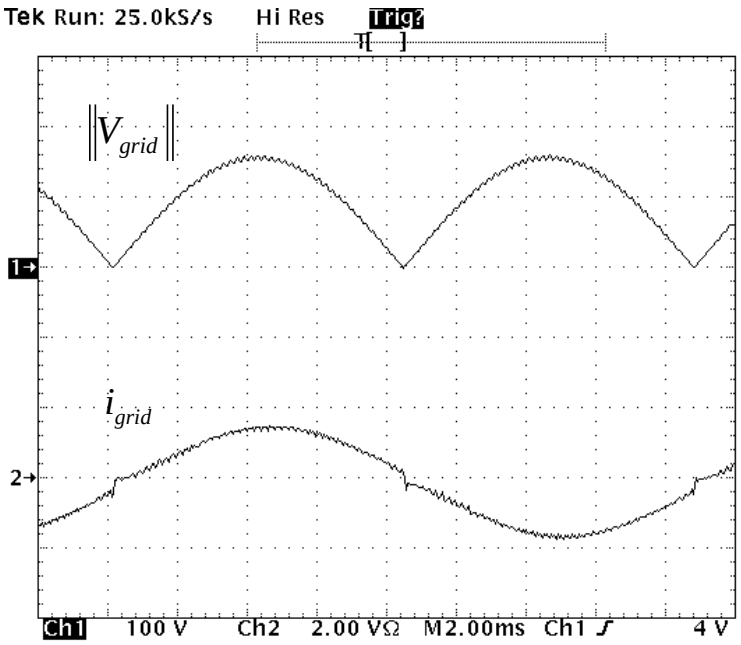


Fig 7.14. Normal operation
V_{pv} =300 V, V_{grid} =110 V_{rms}, P = 120 W
Ch 1: Rectified grid voltage : 100V/DIV, Ch 2: Grid current : 2A/DIV

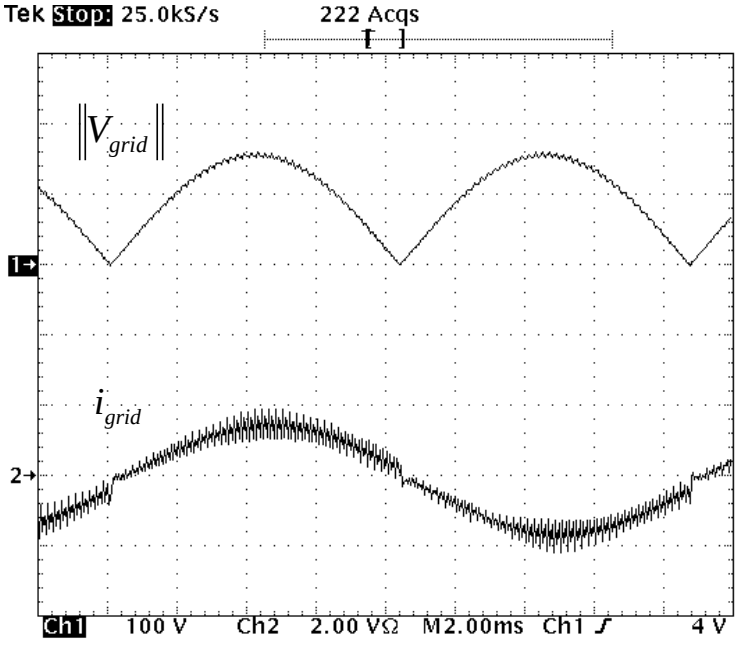


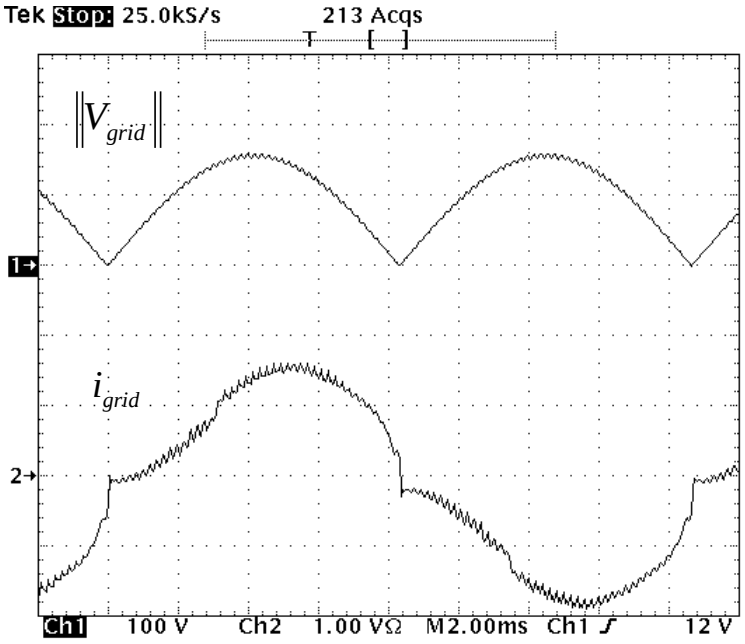
Fig 7.15. Tuning perturbation (10kHz) injection
V_{pv} = 300 V, V_{grid} = 110 V_{rms} , P = 120 W
Ch 1: Rectified grid voltage : 100V/DIV Ch 2: Grid current

For the tuning operation, the perturbation level is set to 5% of the maximum duty cycle command, oscillating at the desired crossover frequency (10 kHz). In the presence of the perturbation, system operation is still stable as shown in Fig 7.15.

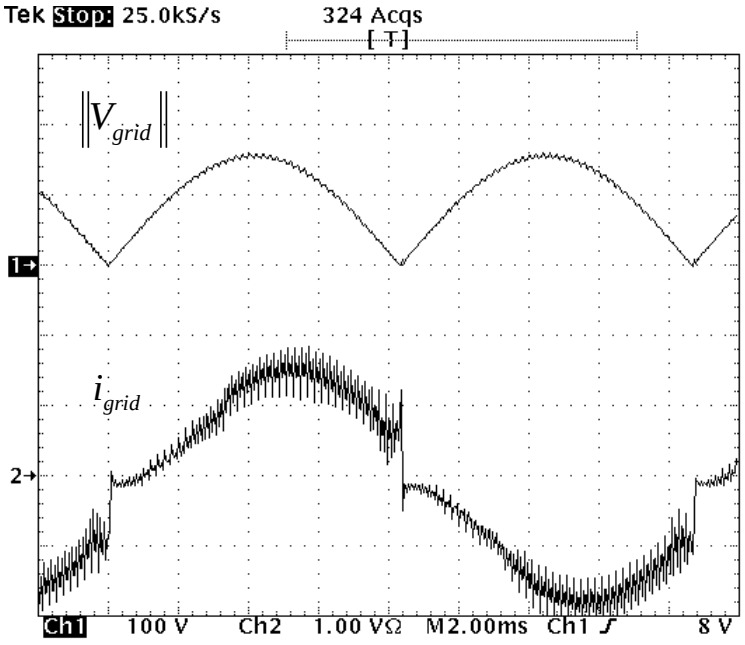
For the purpose of the tuning operation verification, the compensator gain is initially reduced to 1/6 of the nominal compensator gain. When the system is first operated with 1/6 of the nominal gain, it shows fairly distorted waveform as shown in Fig. 7.16(a). Then the perturbation is injected as in Fig. 7.16(b). Tuning is activated to achieve nominal compensator gain as shown in Fig. 7.16(c). After tuning, the grid current is shaped as desired by achieving the nominal compensator gain as shown in Fig. 7.16(d). These tuning results confirm that the tuning technique is applicable to the DC-AC grid-tied inverter system.

7.6 Conclusions and Discussion

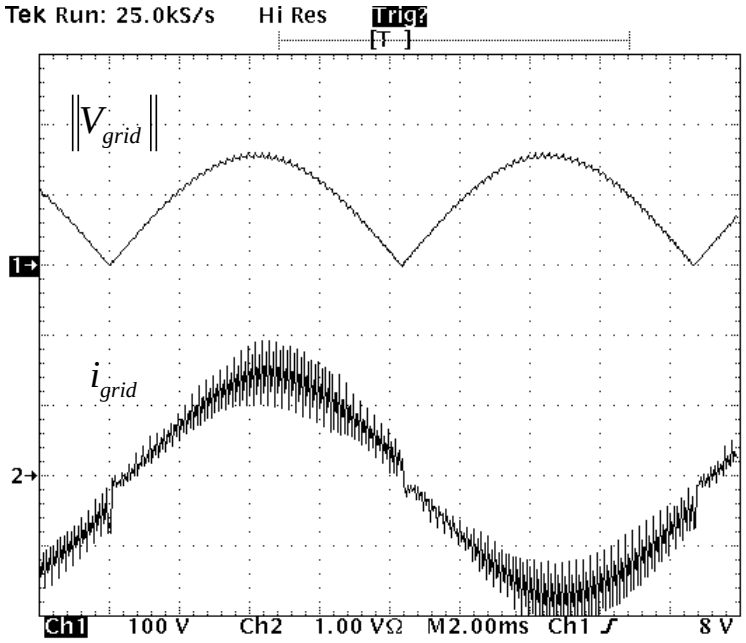
The auto-tuning technique described in Chapters 5 and 6 for AC-DC rectifier systems is applied to the DC-AC grid-tied inverter system. Similarities in the power stage dynamics allow simple tuner application and operation very similar to the AC-DC case. The compensator gain is adjusted to achieve the nominal stability margins in terms of crossover frequency and phase margin in an uncertain situation due to the presence of power stage parameter variations or wrong initial compensator gain. As accomplished in the AC-DC system, the accurate power stage parameter analysis (inductance value) is possible extending the benefits attainable from the auto-tuning technique in the DC-AC grid-tied inverter system.



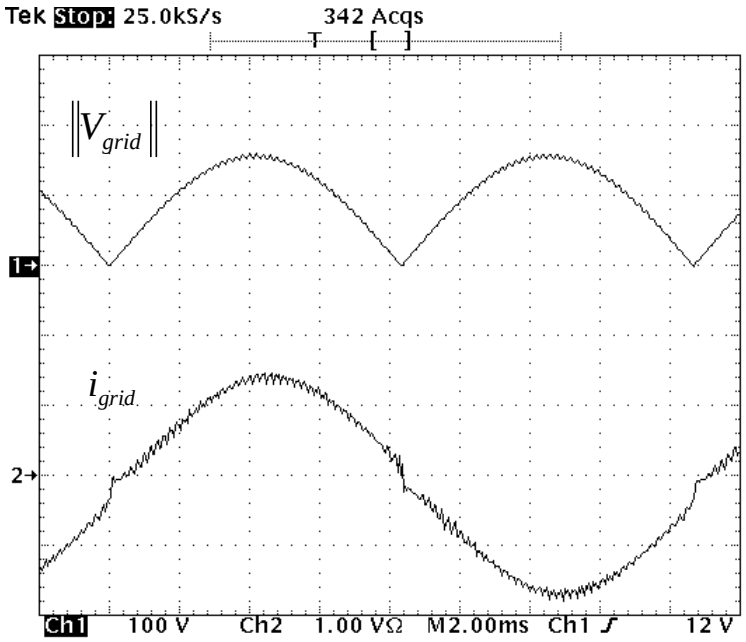
(a) Before tuning (1/6 of nominal compensator gain)



(b) Perturbation is injected



(c) Tuning is activating



(d) After tuning

Fig. 7.16. Current loop tuning procedure
V_{pv} = 300 V, V_{grid} = 110 V_{rms} , P = 120 W
Ch 1: Rectified grid voltage : 100V/DIV Ch 2: Grid current :

CHAPTER 8

Conclusions and Discussion

An auto-tuning technique for high performance digitally controlled single-phase AC-DC rectifiers and grid-tied DC-AC inverters is proposed in the thesis. A sinusoidal perturbation is injected for online power stage parameter estimation, and the compensator parameters are automatically adjusted in such a way that the control loop maintains the pre-determined crossover frequency and the phase margin. Since the tuner only operates based on the injection frequency, tuning operation is not interfered by any other frequency disturbances present in the system. The benefits obtained from the proposed approach can be summarized as follows:

- **Stability Margin Maintenance**

  The power stage tolerances or any other uncertainties can disrupt the system operation by changing the power stage dynamics. This phenomenon is observed in any power conversion modules to different degree. Thus, a smart controller should be designed to adaptively cope with these uncertainties or disturbances. The proposed auto-tuning technique operates by measuring the loop gain at a specific injected frequency. Then, the compensator gain is continuously adjusted to achieve pre-determined cross-over frequency during the tuning process. The phase margin automatically converges to the nominal target value as the cross-

over frequency approaches to the desired value. Since the tuner is activated only for the required period typically less than a few seconds, the injected sinusoidal perturbation does not affect the normal system operation. The auto-tuning technique is capable of stabilizing the system even when the nominal power stage values are not known. The desired cross-over frequency and the phase margin are the only prerequisites for the tuning process.

- **Power Stage Component Value Estimation**

For the stable system operation, it is essential to analyze the accurate value of the power stage component values so that the controller modifies its parameter appropriately. Since the proposed auto-tuning technique directly measures the loop gain magnitude, accurate power stage parameters are available as a result of the tuning process. The precise component values can be very useful in formulating the current programmed control law, which is based on the nominal passive component value.

- **Precise CCM/DCM Boundary Detection**

The adaptive controller, which changes its control strategy properly according to the load status is the core function for the system operating over a wide load range. Generally, the CCM/DCM boundary should be detected using additional circuitry, otherwise the calculation based detection method will lead to erroneous system operation near the boundary due to the tolerances of power stage passive components. With the auto-tuning technique, however, the accurate mode boundary can be calculated by the nominal boundary equation without the cost of additional boundary detection circuitry by taking advantage

of the accurate component values attained during the tuning process. This feature guarantees the stable system operation especially at intermediate loads.

8.1 Future Work

Among the summarized benefits above, the accurate on-line power stage value estimation capability can be further utilized in various ways. In the AC-DC area, the inductor current predictive control techniques have been proposed and being investigated. However, the inductance tolerance disturbs the precise inductor current prediction. In this respect, the accurately estimated inductance by the current loop tuning can provide useful information to the current predictive control technique.

Furthermore, the auto-tuning approach can be further extended to the grid-tied microinverter system [41]. Since one of the critical features of the microinverter is low profile, the passive component size, especially the capacitor size has to be limited in value. Accordingly, the significantly reduced capacitance may possibly invalidate the assumption (7.2), (7.3). As a result, the power stage dynamics derived in (7.5) would not be valid anymore. Consequently, the auto-tuning technique cannot be applied directly in this situation. Hence, appropriate power stage modeling has to be re-examined before the auto-tuning technique is applied in this case.

Appendix A

DC-AC Inverter MATLAB Simulink Simulation

MATLAB Simulink simulation functional block diagrams and the simulation results for digitally controlled DC-AC inverter system are presented. The top system block diagram is shown in Fig A.1. The inverter power stage and the digital averaged current mode controller are implemented together with tuning module. The PV array is assumed to produce 120 W power at 300 V fixed voltage, and the grid voltage is 110 V_{rms}. The inverter power stage parameters are following : L= 400 μH, C= 330 μF, f_{line} = 60 Hz, f_s = 100 kHz, control loop stability margins: φ_m = 55°, f_c= 10 kHz.

Detailed inverter power stage block diagram is shown in Fig A.2, and the top tuning module and the detailed tuning module model are shown in Fig A.3 and Fig A.4 respectively. The simulation result, which verifies the current loop performance is shown in Fig. A.5. The inductor current faithfully tracks the current loop reference as desired. Corresponding duty cycle command waveform and the tuning results are presented in Fig 7.4, and Fig 7.9, Fig 7.10 respectively.

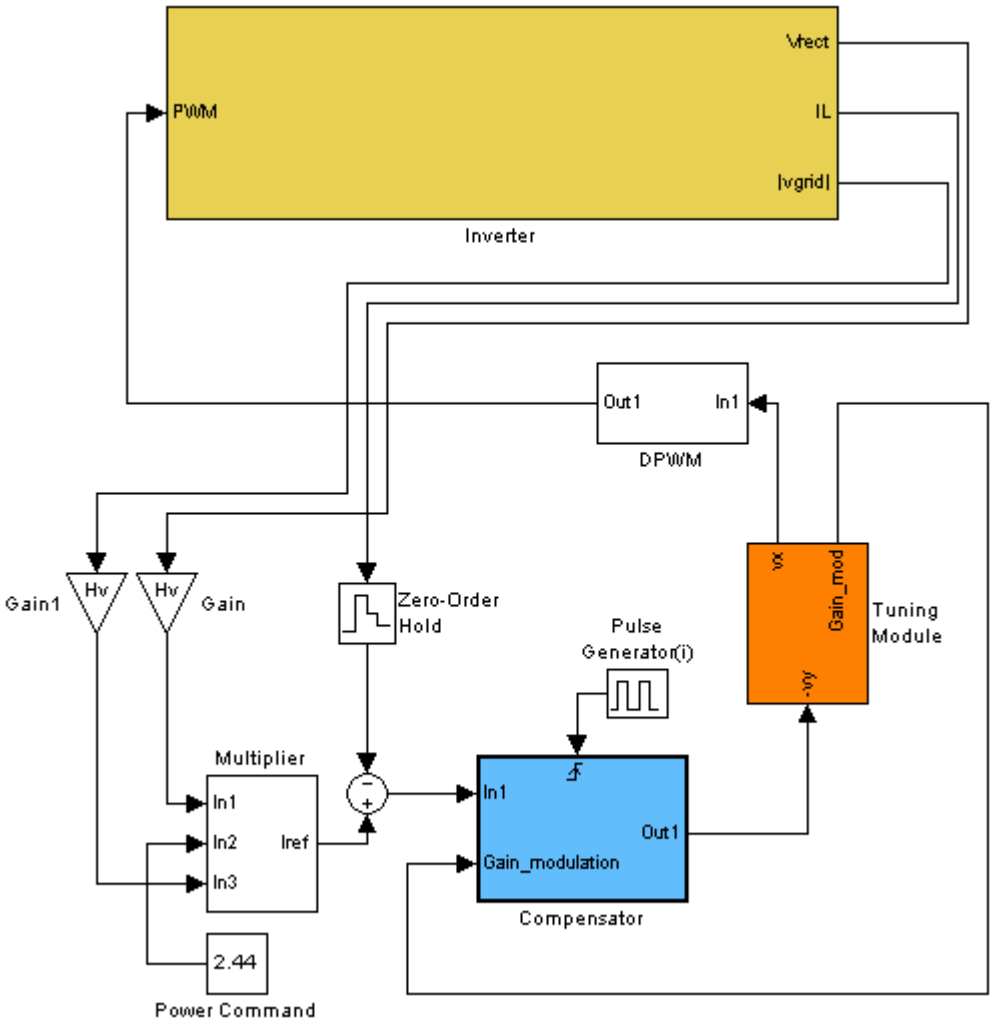


Fig A.1. Grid-tied DC-AC inverter Simulink top block diagram

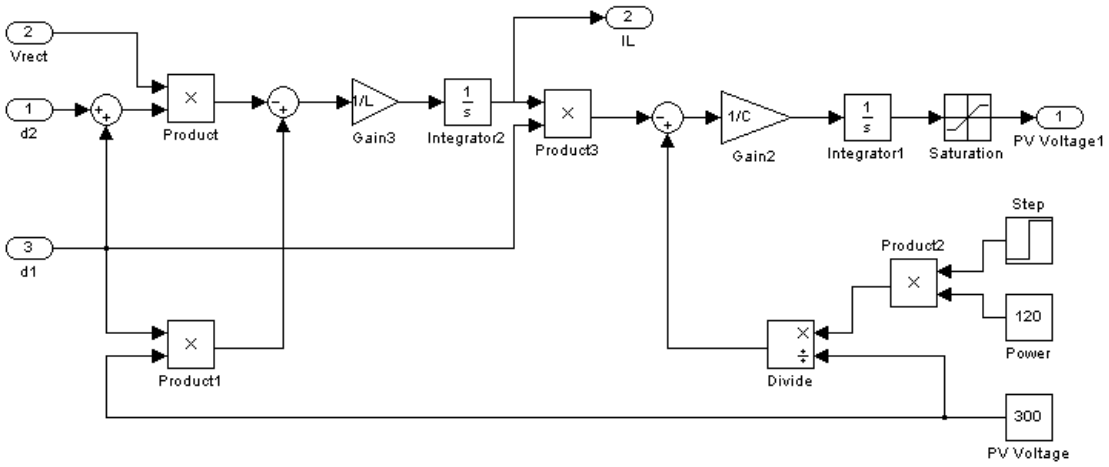


Fig A.2. Grid-tied DC-AC inverter power stage

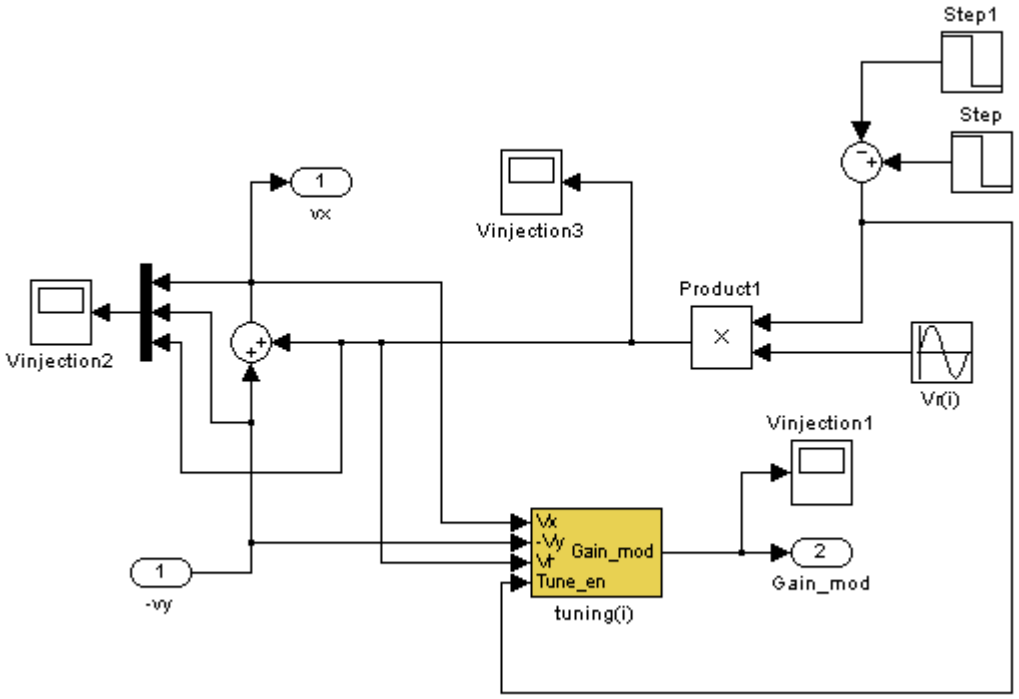


Fig A.3. Tuning module top block diagram

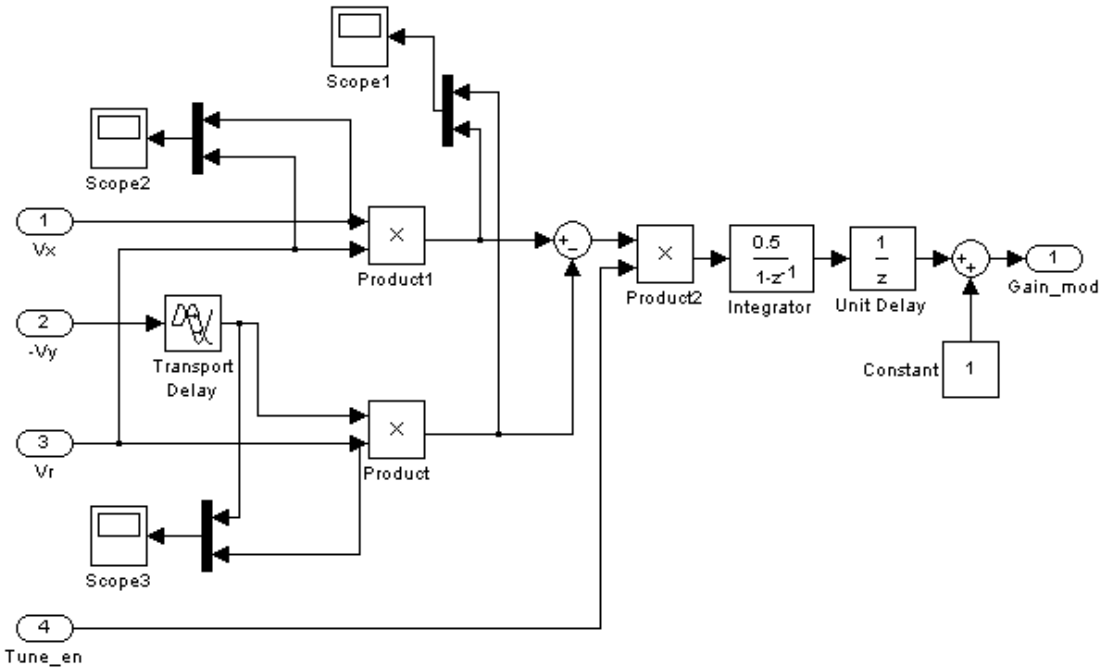


Fig A.4. Detailed tuning module

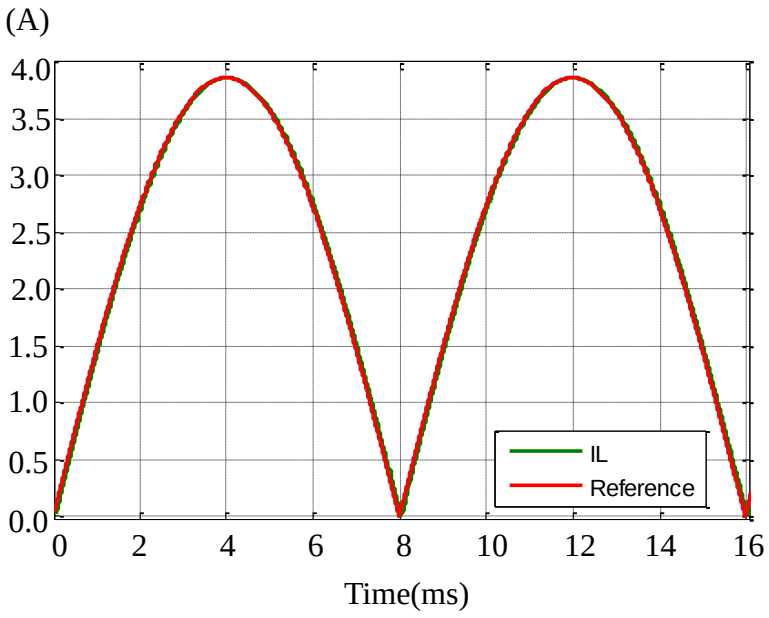


Fig A.5. Current control loop performance (Red: Current loop reference, Green: inductor current)

Current Loop PI Compensator MATLAB Code

```
function [d] = PFC_Gci(e)
persistent yi1 e1 yd1;

if (isempty(yi1))
    yi1 =   0;
    e1  =   0;
    yd1  =  0;

end;

% nominal kp=0.05098
% nominal ki=0.0314
yd = yd1 + 0*(e-e1);
yp  =  (0.05098+e(2))*e(1);
yi =   yi1 + (0.0314+(0.0653753*e(2)))*e(1);
yd  = yd1 + 0*(e(1)-e1);

yi1 =   yi;
e1  =   e;
yd1 =   yd;

d   =   yp + yi + yd;

if (d>1)
    d = 1;
elseif (d<0.02)
    d = 0.00;
end;
```

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